Accurate Level-crossing ADC Design for Biomedical Acquisition Board

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Abstract: The aim of this paper is to present a wireless biomedical system for the acquisition and transmission (Wibio'ACT) of biomedical signals. This work is a part of the Wibio'ACT project which main purpose is to ensure the minimum power consumption while diagnose patients continuously and in real time. For the Wibio'ACT system, the bottleneck is the analog-to-digital conversion (ADC) since it controls the power consumption of the digital signal processing step as well as the amount of the transmitted data. In fact, in this work case, the ADC continuously measures the electrical activity of the heart to deliver the electrocardiogram (ECG) signal. Hence, among conventional ADCs, level-crossing analog-to-digital converters (LC-ADCs) have been investigated for ECG signals processing. Authors propose some design consideration of the LC-ADC. This reduces the LC-ADC output samples by 13 % to help to save the power consumption of the wireless data transmitter. The samples with a small variation are reduced by at least 44%. The performance of the proposed design is measured in terms of percentage root mean square difference (PRD) applied to the reconstructed signal quality. A PRD of 1% is verified using behavioral simulations on ECG records extracted from different databases. A timer period T_C of 0.14 ms ensures an effective number of bits of 10 bits and a signal to noise ratio of 62 dB.

1 INTRODUCTION

In biomedical engineering field, as the cardiovascular diseases are at the top of death causes, many researches focus on the development of reliable and cost effective system for monitoring cardiac patients (Mendis, 2011; Gyselinckx, 2006). One part of these research activities concerns the acquisition, the processing or the wireless transmission of the electrical activity of the heart or any other vital data. Due to the continuous-time monitoring of the patients, large amounts of data need to be processed, stored and transmitted. The key requirements for an efficient high-quality signal monitoring system are power consumption saving, data rate enhancement and distortion robustness.

Therefore, in order to reduce the amount of data after acquisition and before transmission over the radio channels, electrocardiogram (ECG) signal compression requires a lot of attention. Many techniques and algorithms have been proposed including modulation, coding, cosine and wavelet transform (Rajoub, 2002; Cox et al., 1968; Miaou et al., 2005; Ahmed et al., 2009). While many algorithms are deployed for the data compression, few works combine the sampling step to the compression as in level-crossing analog-to-digital converter (LC-ADC) (Mark et al., 1981; Sayiner et al., 1996). In the literature, LC-ADCs are essentially used for audio signal processing particularly speech and ultrasound signals (Allier et al., 2003; Kozmin et al., 2009). In fact, since sampling occurs at irregular times, LC-ADCs are suitable for the conversion of bursty and sparse signals (Guan and Singer, 2007). In the most of the applications, it has been proven that significant performance improvements can be achieved compared to the conventional Nyquist converters in terms of power

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consumption and surface occupation (Kozmin et al., 2009; Guan and Singer, 2007; Li et al., 2013).

In this work, an in-depth study of the main design parameters associated with an LC-ADC is proposed. The present study consists of a detailed analysis of two main parameters that affect the accuracy of the LC-ADC, namely the amplitude resolution and the timer frequency. Additional parameters can also affect the LC-ADC output signal such as the accuracy of the quantization levels and the comparator delay. As a result of this analysis, the authors propose a methodology to select accurate parameters for ECG signals extraction.

To properly present this work, this paper is organized as follows. First, the biomedical smart sensing system architecture is introduced in Section II. Section III describes the LC-ADC architecture. In the same section, the authors present the design considerations for an efficient ECG signal detection to perform both signal compression and power consumption reduction. Section IV presents the results of behavioral simulations on different ECG signals. The percentage root mean square difference (PRD) is used to evaluate signal distortion compared to uniform sampling. Section V concludes the paper.

2 SYSTEM OVERVIEW

The aim of the Wibio'ACT project is to implement a smart system for biomedical signals acquisition and transmission. The two main and innovative topics in this project concern the digitization with an intrinsic compression step via the use of LC-ADC and the reconstruction with a minimum complexity in implementation and a good recovery of the original ECG signal.

2.1 Wibio'ACT System Presentation

The Wibio'ACT system is presented in Figure 1. An acquisition of the biomedical signal is firstly done through the use of non-invasive sensors that wirelessly transmit signal so as to form a wireless body area network (WBAN). The received signal, often a voltage, is amplified and filtered. A classical ADC, SAR (Long et al., 2014) or Sigma-Delta (Giroud et al., 2014) architectures, conventionally performs the digitization of the acquired analog signals. In this project, LC-ADC is chosen thanks to its capacity of compressing the acquired data. This converter allows bypassing the compression of digital data usually ensured by an algorithm implemented on microcontroller. The transmitter is a combination of several functions. They are the mixing stage with a local oscillator (second input of the mixer), as well as the amplification and the filtering stages. At the receiver side, a front end stage composed of functions such as filtering and low noise amplification (LNA) is firstly used. In order to have the original signals, a reconstruction step is necessary to allow the doctor to visualize, analyse and make diagnostics from the biomedical signals.

Besides, the voltage that appears between the sensor electrodes is conditioned via a front-end interface. It includes functions such as amplification using a programmable gain preamplifier (PGA) and analog filtering with passive off-chip filters. For the ECG signal acquisition, a PGA gain of 60 dB is required (Hartmann, 2003). Passive filters including a high-pass filter (HPF) and a low-pass filter (LPF) are composed of capacitors and resistors. The HPF is mainly used to cancel DC-level shift caused by human skin and its cut-off frequency is set to 20 mHz. The LPF is used to eliminate interferers at frequencies above those of ECG signals, so its cut-off frequency is set to 200 Hz. These filtering steps highly influence the reconstruction algorithm performances as any noise would distort their outputs.

The ECG signal acquisition system requires a signal-to-noise ratio (SNR) of at least 61 dB in order to detect heart activities precisely (Li et al., 2013). The ADC to be chosen must have an equivalent effective number of bits approximately equal to 10. As the aim of Wibio'ACT is to enhance transmission and reception of ECG signal with the minimum power consumption, the authors propose the use of LC-ADC. In fact, in this case, the acquisition system exploits the features of the biomedical signals with a small variation (or information) rate to reduce the amount of sampled data. As excepted results, the compression and decompression blocks of the radio modules will be removed and the average speed of the converter will be reduced.

2.2 LC-ADC Principle

An LC-ADC uses level crossing detection to sample the ECG signal after filtering. The converter's architecture shown in Figure 2 consists of two comparators, a digital-to-analog converter (DAC), an up/down counter and a time-to-digital converter (TDC).

Two thresholds levels V^+ and V^- are set to

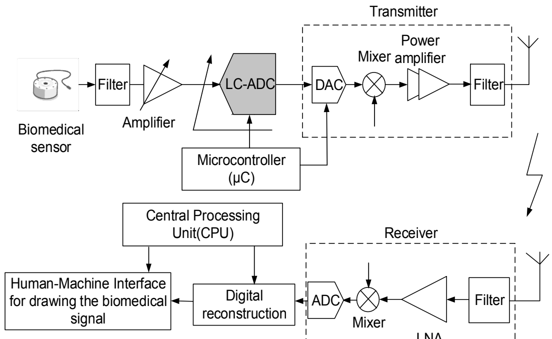


Figure 1: Architecture of Wibio'ACT acquisition board.

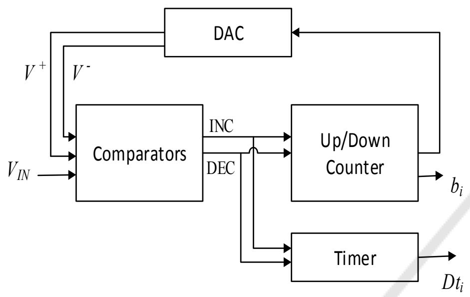


Figure 2: LC-ADC converter architecture.

identify the signal value V_{IN}. These signals are generated via the digital-to-analog converter with a difference equal to the quantization step. Thereby, in digital representation, the difference between V^+ and V^- is equal to 1 LSB. The sampling occurs when the signal value V_{IN} is either higher than V^+ or lower than V^-. In fact, according to the comparison result, the increment signal (INC) or decrement signal (DEC) are exclusively set to "1" and consequently activate the up/down counter. The counter output is either incremented or decremented by 1 LSB. This signal controls the DAC whose generated signals, V^+ and V^-, will be updated to keep tracking the input value. LC-ADC samples are equivalent to the up/down counter output. As long as the signal's value V_{IN} is between V^+ and V^-, INC and DEC are both set to "0" and no changes occurs on the counter or DAC outputs. Thus, no new sample is taken.

The LC-ADC converter adopts $2^M - 1$ levels equally spaced along the input signal range where M is the converter resolution. Samples $(b_i)_{i\in N}$ are generated only when the input signal V_{IN} crosses the defined levels. The time interval, Dt_i , between two consecutive samples is measured by a timer of period T_C. The conversion results of this LC-ADC are thus composed of digital codes, b_i, for the voltage magnitude and the time intervals, Dt_i. The accuracy of data conversion using LC-ADC is dependent on two main factors; the reconstruction condition and the timer frequency.

3 LC-ADC DESIGN CONSIDERATIONS

The LC-ADC samples are non uniformly taken. Thus, the sampling frequency is variable. The number of quantization levels and the signal variations directly influence the number of samples and so the average sampling frequency. Figure 3 presents results of average sampling frequency for different ECG signals when varing the resolution value M. The set of ECG signals used in this simulation is collected through Apnea-ECG Database (apneaecg), combined measurement of ECG Database-Breathing and Seismocardiograms (cebsdb), Long Term ST Database (lgdb), Non-Invasive Fetal ECG Database (nifecdb) and PTB Diagnotic ECG Database (ptbdb) (Moody et al., 2001). The maximum frequency of the ECG signal f_{max} is fixed to 200 Hz to ensure a good quality of ECG parameters detection. The given signals are oversampled and used in digital format in order to emulate an analog signal. The amplitude signal is scaled to the LC-ADC full-scale amplitude. The ECG signal is sampled using the LC-ADC with different resolution values, M. The irregular sampling instants are stored to compute the average sampling frequency.

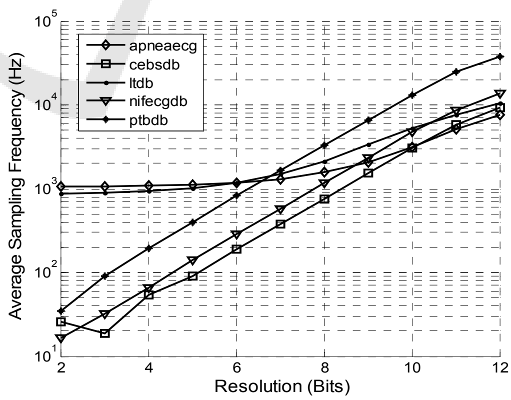


Figure 3: Average sampling frequency versus resolution for ECG signals.

It can be noticed from Figure 3 that the average sampling frequency depends of the LC-ADC resolution M. To satisfy Shannon theorem that imposes the use of a sampling frequency at least equal to the double of the input frequency, the minimum required average sampling frequency is equal to 400 Hz. At this frequency, and according to the input signal, a minimum of 7 bits is needed to recover the original signal after LC-ADC digitization.

The second factor in the LC-ADC design consideration is the timer frequency. Quantization noise is added to the signal due to the inexact time of the sampling instants resulting in jitter noise as presented by Figure 4.

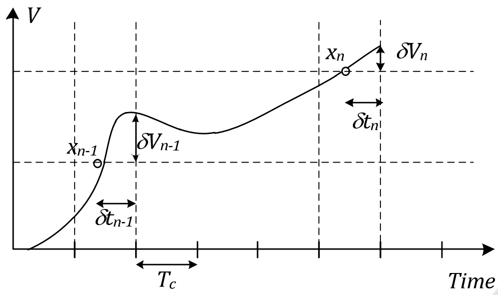


Figure 4: Quantization error due to inexact sampling time.

This error in time, δt, causes an error to the output voltage as in (1), where the derivative of V_{IN} with respect to t is the slope of the input signal.

$$\delta V = \frac{dV_{IN}}{dt}\delta t \tag{1}$$

In this case, the SNR of such system is defined as the ratio of the signal power, computed according to V_{IN} value, to the noise power depending of δV. The theoretical value for the LC-ADC case can be computed as in (2), where T_C is the timer clock period which determines δt (Allier et al., 2003).

$$SNR_{dB} = 10\, log_{10} \frac{12\, P(V_{IN})}{P\left(\frac{dV_{IN}}{dt}\right)} + 20 log_{10}\left(\frac{1}{T_C}\right) \tag{2}$$

According to (2), the SNR no longer depends on the bit resolution of the ADC but instead depends on the timer period T_C and the statistical properties of the input signal V_{IN}. In Figure 5, the SNR and the effective number of bits (ENOB) are plotted versus T_C for ECG signal.

In the irregular sampling scheme, the SNR can be computed from the power density spectrum (PSD) of the reconstructed ECG signal. In this paper, the cubic spline interpolation is the reconstruction algorithm. Doubling the counter frequency results in 6 dB increase of SNR. In fact, to reach an ENOB of 10 bits, a timer frequency of 71 MHz, equivalent to a period T_C of 0.14 µs is considered. Hence, an SNR of 62 dB is ensured by this LC-ADC. From Figure3, with an ENOB equal to 10 bits, the average sampling frequency for the selected database signals is between 3 to 15 kHz.

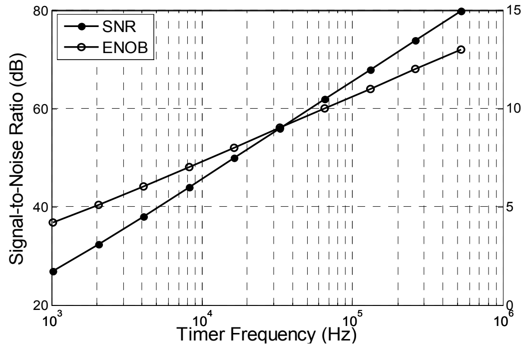


Figure 5: SNR and ENOB versus timer frequency for ECG signal.

Additional factors can influence the performance of the LC-ADC such as the the variation of the comparator delay, the accuracy of the quantization levels and the reconstruction errors due to spline interpolation. Those errors might be taken into account in future work to avoid SNR degradation (Ravanshad et al., 2013).

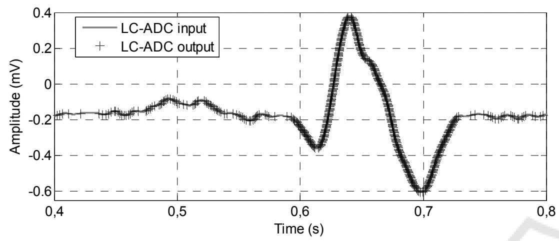
4 SIMULATIONS RESULTS ON ECG SIGNALS

The LC-ADC can compress the sampled data for the same level of performance measured by SNR in case of uniform sampling. It is highly important to accurately choose the design specifications of the converter that are evaluated through the quality of the reconstructed signals. To demonstrate the efficiency of the proposed design in detecting ECG signals, the LC-ADC converter was simulated using a Simulink model for various ECG records obtained from different databases (Moody et al., 2001). The simulation parameters are 0.14 µs for T_C and 10 bits for the resolution M. Since level-crossing is an irregular sampling and in order to use the standard distorsion mesure which is the percentage root mean square difference (PRD), the signal reconstruction based on spline interpolation was performed.

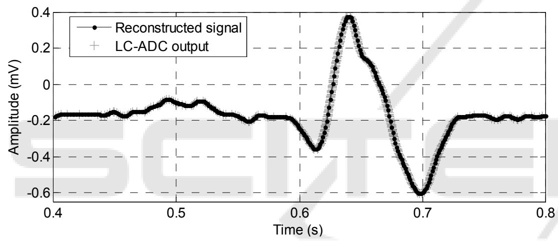
Figure 6 shows the temporal representaion of PTB Diagnotic ECG Database (ptbdb) signal at the input and the output of the LC-ADC. A reconstruction scheme is applied on the output, and presented in the second curve of Figure 6.

In order to measure the signal quality, the PRD of the reconstrcuted signal is measured. The LC-

ADC ensures a PRD of 1%. For a lifestyle application, a PRD value lower than 2% is considered to be adequate as it corresponds to a ‘very good’ reconstruction quality (Zigel et al., 2000). For the same level of SNR and compared to uniform sampling, the LC-ADC compresses the sampled data. As it is show in Figure 7, the LC-ADC reduces the number of low changing voltage sample. In fact, the number of samples representing the small variation between −0.2 and 0 mV are reduced by almost 44%. The total number of samples are reduced by 13%.



(a)



(b)

Figure 6: LC-ADC input and output signals (a) and the reconstructed signal after LC-ADC digitization (b).

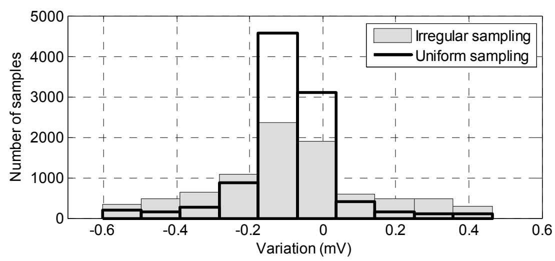


Figure 7: Number of samples in the case of uniform sampling and irregular sampling using LC-ADC.

5 CONCLUSIONS

As demonstrated in this paper, LC-ADC compresses the signal in case of low changing amplitudes. This work investigates the use of LC-ADC to digitize the ECG signals while ensuring an SNR of 62 dB. In fact, it defines the design specification of the LC-ADC converter in order to guarentee a good representation of such vital biomedical signal. To measure the reconstructed signal quality, the PRD parameter is selected. The computed PDR is equal of 1%. Such value is considered to be adequate in biomedical signal processing field. As future work, the LC-ADC circuit implementation can be realized in CMOS process for the proposed values of design specifications. The comparators are hysteretic and can also be implemented as Schmitt triggers. The DACs can be implemented by using the capacitors or the resistor-capacitor hybrid. The digital blocks are simple and can also be designed off-chip.

In addition, future work is necessary to design and implement an adaptive LC-ADC architecture that aims to obtain higher compression rates and more significant power reduction compared to the conventional LC-ADC.

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