

# SEQUENTIAL SYMBOL SYNCHRONIZERS BASED ON CLOCK SAMPLING

Antonio D. Reis<sup>1,2</sup>, Jose F. Rocha<sup>1</sup>, Atilio S. Gameiro<sup>1</sup> and Jose P. Carvalho<sup>2</sup>

<sup>1</sup>Dep. de Electrónica e Telecomunicações / Instituto de Telecomunicações, Universidade de Aveiro, 3810 Aveiro, Portugal

<sup>2</sup>Dep. de Física / U. D. Remota, Universidade da Beira Interior Covilhã, 6200 Covilhã, Portugal

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Abstract: This work presents a sequential symbol synchronizer that was discovered by us, and is based on the clock sampling by the input data transitions. This synchronizer has two types, namely the discrete and the continuous. Each type has two versions which are the manual and the automatic. This synchronizer has an own big advantage, because its manual version adjust hasn't critical phase. The objective is to study the synchronizers and to evaluate their output jitter UIRMS (Unit Interval Root Mean Square) versus input SNR (Signal to Noise Ratio).

## 1 INTRODUCTION

This work studies the sequential symbol synchronizer, based on clock sampling, by the input data transitions.

The input data transitions sample the relative phase of the clock negative transition (Imbeaux, 1983), (Rosenkranz, 1982), (Witte, 1983), (Hogge, 1985), (Simon and Lindsey, 1977).

If this transition clock is delayed then is applied a positive pulse that advances it. However, if the clock is advanced then is applied a negative pulse that delays it (Carruthers, Falconer, Sandler and Strawczynski, 1990), (Huber and Liu, 1992), (D'Amico, D'Andrea and Regianni, 2001), (Dobkin, Ginosar and Sotiriou, 2004), (Noels, Steendam and Moeneclaey, 2006).

The clock positive transition samples the data at the symbols center (maximum opening eye diagram). We present two types/ variants of synchronizers each one with two versions.

Fig.1 shows the functioning principle of the referred synchronizers.

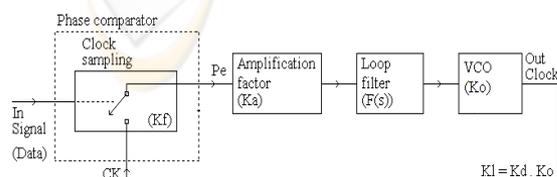


Figure 1: Aspect of the synchronizer based on clock sampling.

$K_f$  is the phase comparator gain,  $F(s)$  is the loop filter,  $K_o$  is the VCO gain and  $K_a$  is the loop amplification that controls the root locus and the loop desired characteristics.

Following, we present the discrete synchronizer with its versions manual and automatic.

Next, we present the continuous synchronizer with its versions manual and automatic.

After, we present the design and tests.

Then, we present the results.

Finally, we present the conclusions.

## 2 DISCRETE SYNCHRONIZER TYPES

The discrete type has a pulse error  $P_e$  that goes discretely to the equilibrium point, without to disappear. This discrete type has the following versions manual and automatic (Reis, Rocha, Gameiro and Pacheco, 2008).

### 2.1 Discrete Type and Manual Version

The manual version is based on a delay line that needs a previous human adjustment. This delay determines the charge pulse area (Fig.2).

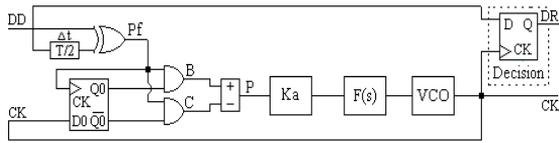


Figure 2: Synchronizer discrete and manual (d-m).

The exor with delay  $T/2$  produces a fixed pulse  $P_f$  that determines the charge rhythm.

Fig.3 shows the waveforms of the synchronizer discrete and manual.

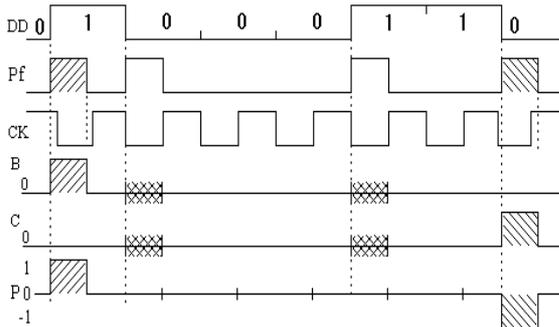


Figure 3: Waveforms of the synchronizer discrete and manual.

The error pulse  $P_e$  maintains its area in synchronization and remains constant at the equilibrium point (Reis, Rocha, Gameiro and Pacheco, 2008).

### 2.2 Discrete Type and Automatic Version

The automatic version is based on a flip flop that automatically provides the delay. This delay determines the charge pulse area (Fig.4).

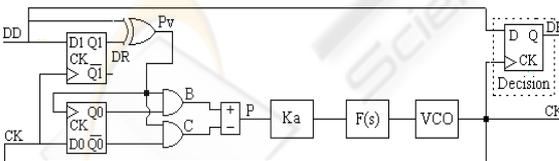


Figure 4: Synchronizer discrete and automatic (d-a).

The flip flop 1 with produces a variable pulse  $P_v$  that determines the charge rhythm.

Fig.5 shows the waveforms of the synchronizer discrete and automatic.

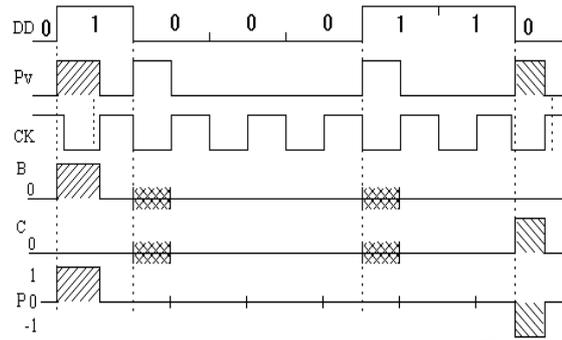


Figure 5: Waveforms of the synchronizer discrete and automatic.

The error pulse  $P_e$  varies its area in synchronization, but remains more or less constant at the equilibrium point.

## 3 CONTINUOUS SYNCHRONIZER TYPES

The continuous type has a pulse error that goes continuously to the equilibrium point and disappear. This continuous type has the following versions manual and automatic (Reis, Rocha, Gameiro and Pacheco, 2008).

### 3.1 Continuous Type and Manual Version

The manual version is based on a delay line that needs a previous human adjustment. This delay determines the charge pulse area (Fig.6).

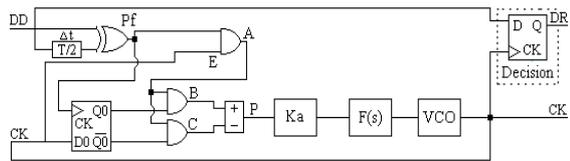


Figure 6: Synchronizer continuous and manual (c-m).

The exors with delay  $T/2$  and AND A produces a variable pulse A that determines the charge rhythm.

Fig.7 shows the waveforms of the synchronizer continuous and manual.

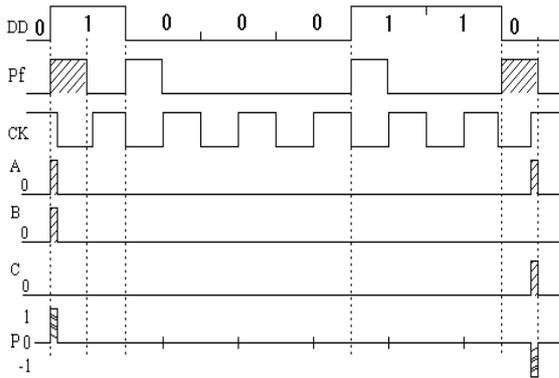


Figure 7: Waveforms of the synchronizer continuous and manual.

The error pulse  $P_e$  diminishes its area in synchronization and disappear at the equilibrium point.

### 3.2 Continuous Type and Automatic Version

The automatic version is based on a flip flop that automatically provides the delay. This delay determines the charge pulse area (Fig.8).

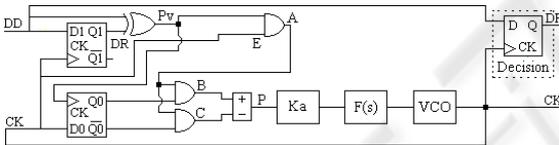


Figura 8: Synchronizer continuous and automatic (c-a).

The exors with delay  $T/2$  and AND A produces a variable pulse A that determines the charge rhythm.

Fig.9 shows the waveforms of the synchronizer continuous and automatic.

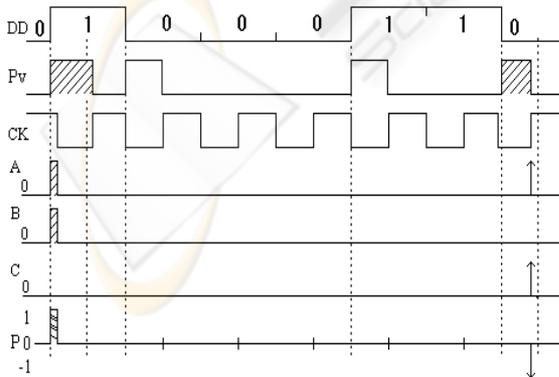


Figure 9: Waveforms of the synchronizer continuous and automatic.

The error pulse  $P_e$  diminishes its area in synchronization and disappear at the equilibrium point.

## 4 DESIGN, TESTS AND RESULTS

We will present the design, tests and results of the referred synchronizers (Reis, Rocha, Gameiro and Pacheco, 2001).

### 4.1 Design

To get guaranteed results, it is necessary to dimension all the synchronizers with equal conditions. Then it is necessary to design all the loops with identical linearized transfer functions.

The general loop gain is  $Kl=Kd.Ko=Ka.Kf.Ko$  where  $Kf$  is the phase comparator gain,  $Ko$  is the VCO gain and  $Ka$  is the control amplification factor that permits the desired characteristics.

For analysis facilities, we use a normalized transmission rate  $t_x=1$ baud, what implies also normalized values for the others dependent parameters. So, the normalized clock frequency is  $f_{CK}=1$ Hz.

We choose a normalized external noise bandwidth  $B_n = 5$ Hz and a normalized loop noise bandwidth  $B_l = 0.02$ Hz. Later, we can disnormalize these values to the appropriated transmission rate  $t_x$ .

Now, we will apply a signal with noise ratio SNR given by the signal amplitude  $A_{ef}$ , noise spectral density  $N_o$  and external noise bandwidth  $B_n$ , so the  $SNR = A_{ef}^2 / (N_o \cdot B_n)$ . But,  $N_o$  can be related with the noise variance  $\sigma_n$  and inverse sampling  $\Delta\tau=1/Samp$ , then  $N_o=2\sigma_n^2 \cdot \Delta\tau$ , so  $SNR=A_{ef}^2 / (2\sigma_n^2 \cdot \Delta\tau \cdot B_n) = 0.5^2 / (2\sigma_n^2 \cdot 10^{-3} \cdot 5) = 25 / \sigma_n^2$ .

After, we observe the output jitter  $UI$  as function of the input signal with noise SNR. The dimension of the loops is:

- 1<sup>st</sup> order loop:

The loop filter  $F(s)=1$  with cutoff frequency 0.5Hz ( $B_p=0.5$  Hz is 25 times bigger than  $B_l=0.02$ Hz) eliminates only the high frequency, but maintain the loop characteristics.

The transfer function is

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{KdKoF(s)}{s + KdKoF(s)} = \frac{KdKo}{s + KdKo} \quad (1)$$

the loop noise bandwidth is

$$Bl = \frac{KdKo}{4} = Ka \frac{KfKo}{4} = 0.02Hz \quad (2)$$

Then, for the analog synchronizers, the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4 \quad \text{with } (Km=1, A=1/2, B=1/2; Ko=2\pi)$$

$$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2/\pi \quad (3)$$

For the hybrid synchronizers, the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4 \quad \text{with } (Km=1, A=1/2, B=0.45; Ko=2\pi)$$

$$(Ka.Km.A.B.Ko)/4 = 0.02 \rightarrow Ka=0.08*2.2/\pi \quad (4)$$

For the combinational synchronizers, the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4 \quad \text{with } (Kf=1/\pi; Ko=2\pi)$$

$$(Ka*1/\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.04 \quad (5)$$

For the sequential synchronizers, the loop bandwidth is

$$Bl=0.02=(Ka.Kf.Ko)/4 \quad \text{with } (Kf=1/2\pi; Ko=2\pi)$$

$$(Ka*1/2\pi*2\pi)/4 = 0.02 \rightarrow Ka=0.08 \quad (6)$$

The jitter depends on the RMS signal  $A_{ef}$ , on the power spectral density  $No$  and on the loop noise bandwidth  $Bl$ .

For analog PLL the jitter is:

$$\sigma\phi^2 = Bl.No/A_{ef}^2 = Bl.2.\sigma n^2.\Delta\tau = 0.02*10^{-3} * 2\sigma n^2/0.5^2 = 16*10^{-5}.\sigma n^2$$

For the others PLLs the jitter formula is more complicated.

- 2<sup>nd</sup> order loop:

The second order loop is not shown here, but the results are identical to the ones obtained above for the first order loop.

## 4.2 Tests

The following figure (Fig.10) shows the setup that was used to test the various synchronizers.

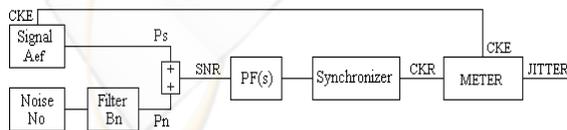


Figure 10: Block diagram of the test setup.

The receiver recovered clock with jitter is compared with the emitter original clock without jitter, the difference is the jitter of the received clock.

## 4.3 Jitter Mesurer (Meter)

The jitter mesurer (Meter) consists of a RS flip flop, which detects the random variable phase of the recovered clock (CKR), relatively to the fixed phase of the emitter clock (CKE). This relative random phase variation is the recovered clock jitter (Fig.11).

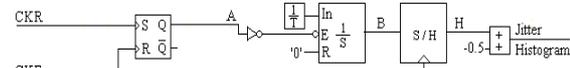


Figure 11: The jitter mesurer (Meter).

The other blocks convert this random phase variation into a random amplitude variation, which is the jitter histogram.

Then, the jitter histogram is sampled and processed by an appropriate program, providing the RMS jitter and the peak to peak jitter.

## 4.4 Results

We will present the results (output jitter UIRMS versus input SNR) for the four synchronizers.

Fig.12 shows the jitter-SNR curves of the four synchronizers: discrete and manual (d-m), discrete and automatic (d-a), continuous and manual (c-m) and continuous and automatic (c-a).

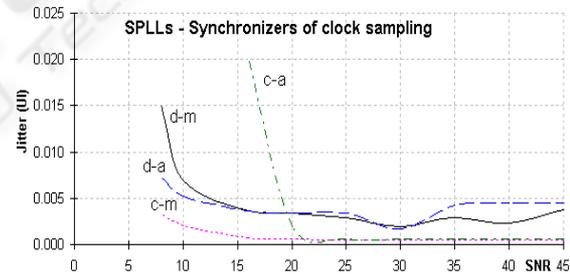


Figure 12: Jitter-SNR curves of the four synchronizers(d-m,d-a,c-m,c-a).

We verify, that generally the output jitter UIRMS diminishes gradually with the input SNR increasing.

For high SNR, the four curves tend to be equals, but with some disadvantage of the discrete automatic (d-a). However, for low SNR the continuous manual (c-m) is the best, followed of the discrete manual (d-m). After is the discrete automatic (d-a) and at last the continuous automatic (c-a).

## 5 CONCLUSIONS

We studied four synchronizers, namely the discrete manual (d-m), the discrete automatic (d-a), the continuous manual (c-m) and the continuous automatic (c-a). Then, we tested their output jitter UIRMS versus input SNR.

We observed that, generally, the jitter UIRMS diminishes gradually with the SNR increasing.

We verified, that for high SNR, the jitter of the four synchronizers is similar, but with a slight disadvantage of the discrete automatic (d-a). This is comprehensible since the error pulse  $P_e$  is variable and don't disappear at the equilibrium point.

However, for low SNR, the continuous manual (c-m) is the best, this is comprehensible since the error pulse  $P_e$  diminishes gradually and disappear at the equilibrium point, also the additional AND is a closed door to the noise. The discrete automatic (d-a) and the discrete automatic (d-a) have an intermedium performance since their error pulse  $u$  don't disappear at the equilibrium point. The continuous automatic (c-a) has the worst jitter, since its error pulse  $P_e$  has non symmetric positive and negative pulse contributions that aggravates the jitter.

## ACKNOWLEDGEMENTS

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## REFERENCES

- Imbeaux, J. C., 1983. Performance of the delay-line multiplier circuit for clock and carrier synchronization. *IEEE Journal on Selected Areas in Communications* p.82 Jan.
- Rosenkranz, W., 1982. Phase Locked Loops with limiter phase detectors in the presence of noise. *IEEE Trans. on Communications* com-30 N°10 pp.2297-2304. Oct.
- Witte, H. H., 1983. A Simple Clock Extraction Circuit Using a Self Sustaining Monostable Multivibrator Output Signal. *Electronics Letters*, Vol.19, Is.21, pp.897-898, Oct.
- Hogge, C. R., 1985. A Self Correcting Clock Recovery Circuit. *IEEE Tran. Electron Devices* p.2704 Dec.
- Reis, A. D., Rocha, J. F., Gameiro, A. S., Carvalho, J. P., 2001. A New Technique to Measure the Jitter. Proc. *III Conf. on Telecommunications* pp.64-67 FFoz-PT 23-24 Apr.
- Simon, M. K., Lindsey, W. C., 1977. Tracking Performance of Symbol Synchronizers for Manchester Coded Data. *IEEE Transactions on Communications* Vol. com-25 N°4, pp.393-408, April.
- Carruthers, J., Falconer, D., Sandler, H., Strawczynski, L., 1990. Bit Synchronization in the Presence of Co-Channel Interference. Proc. *Conf. on Electrical and Computer Engineering* pp.4.1.1-4.1.7, Ottawa-CA 3-6 Sep.
- Huber, J., Liu, W., 1992. Data-Aided Synchronization of Coherent CPM-Receiver. *IEEE Transactions on Communications* Vol.40 N°1, pp.178-189, Jan.
- D'Amico, A., D'Andrea, A., Reggianni, 2001. Efficient Non-Data-Aided Carrier and Clock Recovery for Satellite DVB at Very Low SNR. *IEEE Jou. on Satellite Areas in Comm.* Vol.19 N°12 pp.2320-2330, Dec.
- Dobkin, R., Ginosar, R., Sotiriou, C. P., 2004. Data Synchronization Issues in GALS SoCs. Proc. *10th International Symposium on Asynchronous Circuits and Systems*, pp.CD-Ed., Crete-Greece 19-23 Apr.
- Noels, N., Steendam, H., Moeneclaey, M., 2006. Effectiveness Study of Code-Aided and Non-Code-Aided ML-Based Feedback Phase Synchronizers. Proc. *IEEE Int Conf. on Comm.(ICC'06)* pp.2946-2951, Ist.-TK, 11-15 Jun.
- Reis, A. D., Rocha, J. F., Gameiro, A. S., Carvalho, J. P., 2008. The Electromagnetic Wave and the Principle of the Telecommunications. Proc. *VI Sym. on Enabling Optical Network and Sen. (SEONs 2008)* p.87-88, Av-PT 29-29 Jun.