A New Architecture Proposal of Half-wave Precision Rectifier using a Single VCII

Leila Safari[1,2][a], Gianluca Barile[1,2][b], Mattia Ragnoli[1][c], Giuseppe Ferri[1][d] and Vincenzo Stornelli[1,2][e]

[1]*Department of Industrial and Information Engineering, University of L'Aquila, Italy Località Campo di Pile, via Gronchi 18, L'Aquila 67100, Italy*

[2]*DEWS research center, University of L'Aquila, Italy Località Campo di Pile, via Gronchi 18, L'Aquila 67100, Italy*

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Abstract: In this paper a new second generation voltage conveyor (VCII) based half wave rectifier circuit architecture proposal is presented. Both inverting and non-inverting outputs in the form of voltage signal are produced. The proposed circuit is the first half wave rectifier architecture using VCIIs introduced in the literature. It consists of one VCII, two diodes and a single grounded resistor. The input signal is in current form and the rectified output voltage signal is provided at the low impedance Z port of the same VCII. Therefore, the produced output signal can be directly used with no need to add extra voltage buffers. In addition, the circuit gain is set by the grounded resistor value and can be tuned. The proposed circuit enjoys a simple transistor-level structure employing only 21 transistors. In this paper, the architecture of the rectifier is presented and explained, as well as a possible VCII topology. Preliminary simulation results are also given highlighting its capabilities. Its simplicity and versatility make it suitable for sensor interfaces and processing circuits for sensor networks where a low power consumption for the analog processing section is of the utmost importance.

1 INTRODUCTION

Circuits converting alternating signals to direct signals are basic building blocks used in various signal processing fields such as applications requiring RMS to DC conversion, AC voltmeters, low level signal conditioning, measurement, instrumentation etc. (Toumazou et al., 1987). Figure 1 shows the traditional operational amplifier (OA) based half wave precision rectifier realization (Samyhosny et al., 1994). There are two main advantages for the circuit of Fig.1.

First, the rectified output signal can be directly used because the rectified output is provided in the form of voltage signal at low impedance output port of OA. Second, OA also reduces the problem of diode cut-in voltage. However, the conventional OA based half wave rectifier of Fig.1 is limited to operate well below OA gain bandwidth product (GBW) and hence it is not suitable for high frequency applications. More importantly, there is large distortion in the output signal in zero crossing due to the finite slew rate of OA. The problems associated with conventional OA based rectifier is effectively solved using current mode approach. Several precision rectifiers based on current mode active building blocks have been reported in open literature (Kumngern, 2009; Virattiya et al., 2011; Kumngern, 2010; Monpapassorn et al., 2001; Oruganti et al., 2017; Lidgey et al. 1993; Kumar et al.; 2020; Sagbas

[a] https://orcid.org/0000-0003-0863-5660
[b] https://orcid.org/0000-0003-4937-0398
[c] https://orcid.org/0000-0002-1536-3969
[d] https://orcid.org/0000-0002-8060-9558
[e] https://orcid.org/0000-0001-7082-9429

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et al; 2016; Hirunporm et al.; 2021). The possibility of driving diodes by high output impedance current sources which eliminates the problems caused by limited slew rate of OAs as well as inherent high frequency

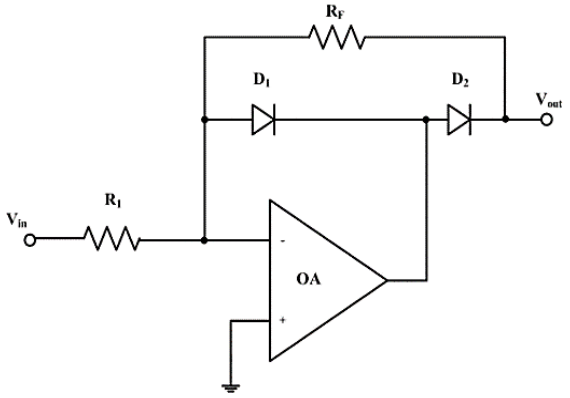


Figure 1: OA based half wave rectifier (Samyhosny et al., 1994).

performance of current mode active building block are two main motivations in realizing various current mode precision rectifiers.

Literature survey shows that current mode signal processing has been helpful in overcoming the issues related to OA based precision rectifiers. However, current mode precision rectifiers suffer from a great weakness in applications where rectified output signal is required in voltage form. This is mainly because most of current mode active building blocks lacks a low impedance voltage output port. For example, in (Kumngern, 2009) a voltage output half wave rectifier is presented. It employs a voltage to current converter and 21 MOS transistors. The circuit requires extra voltage buffer at output for practical use. In (Virattiya et al., 2011) a half-wave rectifier using a current comparator and two current mirrors is presented. The output signal is in the form of current. The half-wave rectifier reported in (Kumngern, 2010) employs an operational trans-resistance amplifier (OTA), two diodes, one reference voltage and one grounded resistor. The half-wave rectifier of (Monpapassorn et al., 2001) employs an I-V converter, half wave rectifier, and a V-I converter. In (Oruganti et al., 2017) a voltage output half-wave rectifier based on two OTA, five resistors, one bias voltage and 6 MOS transistors is reported. However, all the aforementioned solutions suffer from inappropriate impedance at output node and for practical use, voltage buffer is required.

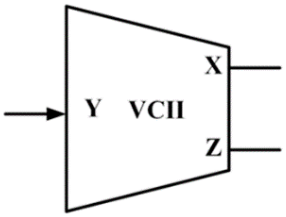
Recently, a new active building block called second generation voltage conveyor (VCII) (Safari et al., 2019a, 2019b) that shows a low impedance voltage output port, has gained great interest for applications requiring voltage signals. Literature study shows that VCII can be used in many applications such as: analog interface circuit for capacitive sensors (Barile et al., 2019a), SiPM interface circuit (Ferri et al., 2021), instrumentation (Safari et al., 2021), multiplying circuit for low value capacitive sensors (Stornelli et al., 2021) etc. More importantly, VCII application as a voltage output full wave precision rectifier has been reported recently (Safari et al., 2020). In this paper we propose a new architecture for VCII based voltage output half wave precision rectifier implementation. The proposed topology employs only one VCII, two diodes and one grounded resistor. Both inverting and non-inverting outputs can be provided at low impedance Z port of VCII. The overall gain can be simply set by resistor value. The organization of this paper is as follows: in section 2 proposed circuit architecture is discussed. Section 3 describes the transistor level architecture of the implemented VCII. Lastly, section 4 draws some conclusions.

2 PROPOSED ARCHITECTURES

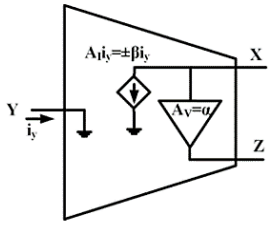
Figure 1 shows the VCII symbol and the internal structure. As it is shown, it consists of a current buffer and a voltage buffer. Y is low impedance current input port, X is high impedance current output port and Z is low impedance voltage output port. The operation of VCII is described as:

$$i_x = \pm\beta i_y, V_z = \alpha V_x \quad (1)$$

where β is current gain between Y and X terminals and α is voltage gain between X and Z terminals. The ideal values of β and α are unity. The + and – signs indicate VCII+ and VCII- respectively. The parasitic impedances at Y, X and Z terminals (r_Y, r_X and r_Z respectively) in ideal case are zero, infinite and zero respectively. The proposed VCII- based half wave positive and negative rectifiers are shown in Fig.3a and Fig.3b respectively



(a)



(b)

Figure 2: The VCII: a) schematic diagram b) symbolic representation (Safari et al., 2019a).

They are based on two diodes, one grounded resistor and one VCII- as active element. The input signal is in current form and the produced rectified output signal is in voltage form. For Fig.3a, by ignoring parasitic impedances, its operation can be described as follows: for $I_{in} > 0$, D_1 is off and D_2 is on, and we have:

$$I_y = I_{in} \tag{2}$$

From eq.(1), we have:

$$I_x = -\beta I_y = -\beta I_{in} \tag{3}$$

Using eq.(3) and eq.(1), V_{out} is found as:

$$V_{out} = \alpha\beta R_1 I_{in} \tag{4}$$

For $I_{in} < 0$, D_1 is on and D_2 is off, and we have:

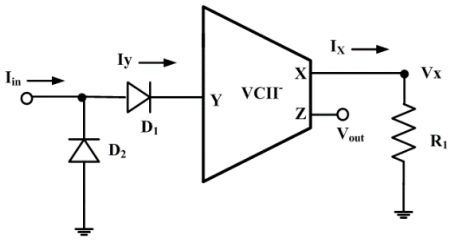
$$I_y = 0, I_x = 0 \; and \; V_x = 0 \tag{5}$$

Therefore, the operation of the proposed positive VCII- based half wave rectifier can be expressed as:

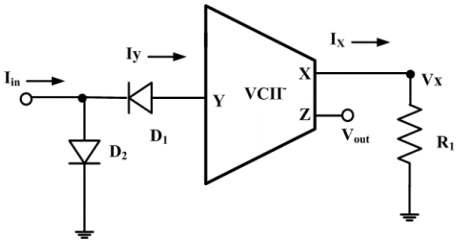
$$V_{out} = \begin{cases} V_{out} = \alpha\beta R_1 I_{in} & I_{in} > 0 \\ 0 & I_{in} < 0 \end{cases} \tag{6}$$

As it is seen from eq.(6), the circuit gain can be set by R_1 value.
The proposed negative half wave rectifier is shown in Fig.3b. Similarly, its operation is expressed as:

$$V_{out} = \begin{cases} 0 & I_{in} > 0 \\ V_{out} = \alpha\beta R_1 I_{in} & I_{in} < 0 \end{cases} \tag{7}$$

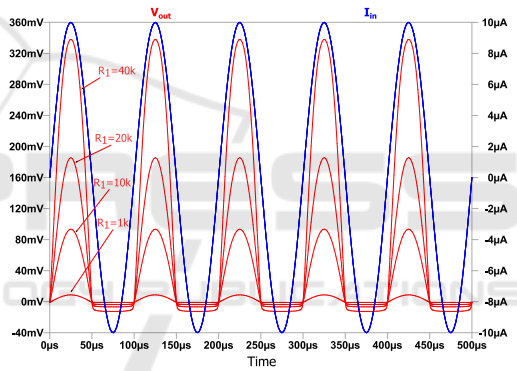


(a)

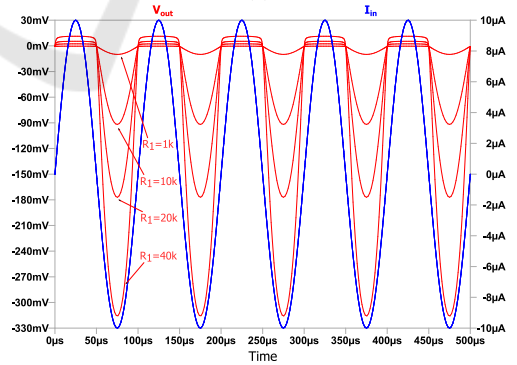


(b)

Figure 3: Proposed a) positive and b) negative half wave rectifiers.



(a)



(b)

Figure 4: Time domain analysis of the a) positive and b) negative half wave rectifiers.

Figure 4 shows an example of time domain behavior of the positive (Fig.4a) and negative (Fig.4b) rectifiers. The VCII topology used for these simulations is reported in Section 4, while the used diodes are 1PS79SB63 (Datasheet 1PS79SB63, 2004). The input signal is a sinusoidal wave with an amplitude of 10 µA and a frequency of 10 kHz. The output voltage is reported at different values of R_1: 1 kΩ, 10 kΩ, 20 kΩ and 40 kΩ.

3 VCII INTERNAL TOPOLOGY

The CMOS implementation of the VCII- is shown in Fig.5. A current buffer made of transistors M_1-M_9 transfer Y port input current to X node. The voltage produced at X node is conveyed to Z port by means of a voltage buffer realized by M_{10}-M_{14}. Transistors M_{B1}-M_{B6} are used for biasing purpose.

The circuit was designed using AMS 0.35 µm technology, with a ±1.65 V supply voltage. The total power consumption is 600 µW.

Simulation results concerning the main VCII parameters are reported in Fig. 6 and Fig. 7. Specifically, Fig. 6 shows the two parameters α and β, where the value is equal to 0.995 and 0.975 respectively. Terminal impedances are shown in Fig. 7: at X node the high impedance equals 1.65 MΩ, whereas at the low impedance nodes Y and Z there are 50 Ω and 87 Ω, respectively

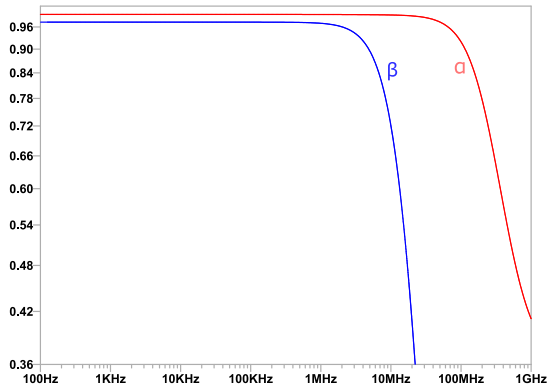


Figure 6: VCII- α and β parameters.

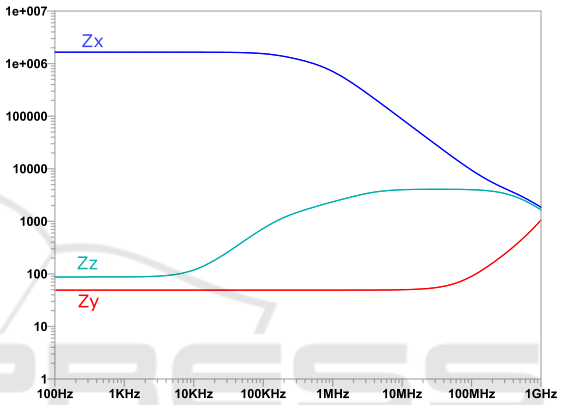


Figure 7: VCII- impedances.

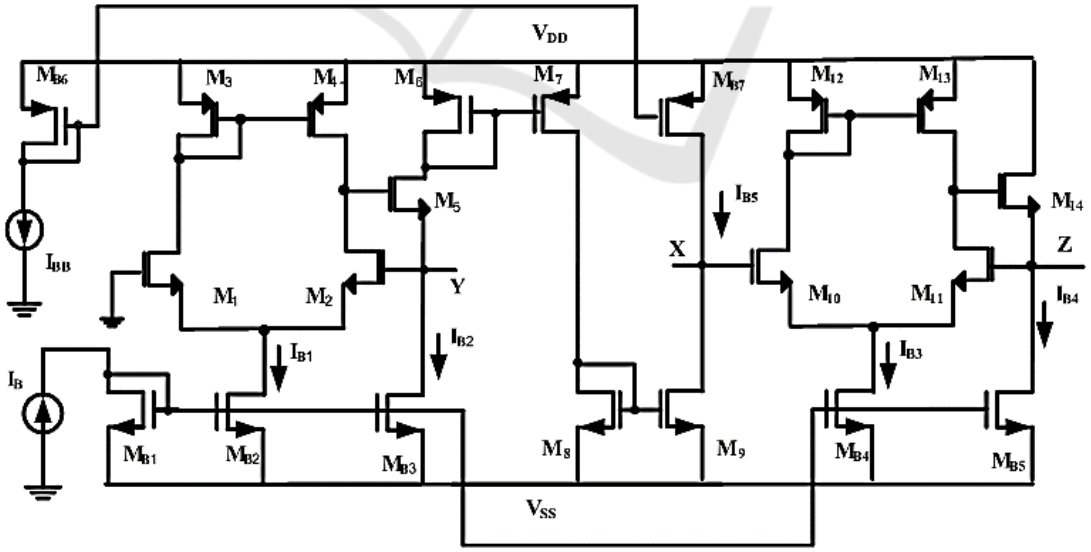


Figure 5: CMOS implementation of VCII-.

4 CONCLUSIONS

A new circuit topology for realizing inverting and non-inverting half wave rectifiers is presented. Only one VCII-, two diodes and a single resistor are used. The circuit gain can be adjusted by resistor value. The input signal is in current form and rectified output signal is in voltage form which is provided in low impedance Z port of VCII-. Therefore, no voltage buffer is required for practical application. Simple implementation, high frequency performance, low power consumption and low linearity error are main advantages of the proposed half wave rectifier topology.

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