

# Detection of $<12 \mu\text{V}_{\text{RMS}}$ Extracellular Action Potential and Local Field Potential by Optimum Design of a Single Pixel Electrolyte-Oxide-MOSFET Interface in CMOS 28 nm

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**Abstract:** Microelectrode-Arrays (MEAs) allow monitoring thousands of neurons/mm<sup>2</sup> by sensing: extracellular Action Potentials and (in-vivo) Local Field Potentials. MEAs arrange several recording sites (or pixels) in a spatial grid, planarly and capacitively coupled with in-vitro cell cultures and/or integrated in electrocorticography grids. This paper focuses on Electrolyte-Oxide MOS Field-Effect-Transistors (EOMOSFET) MEAs for cell-level recording and presents a complete model of the neuron-electronics junction that reduces to a single electrical scheme all the biological (the neuron) and physical layers (the electrolyte, the Diffuse/Helmoltz capacitances, the oxide and the MOS transistor) composing the interface. This allows to predict the noise power coming from biological environment (electrolyte bath) and to optimize all electrical parameters with the main aim to minimize the final sensing Noise Figure and thus enhance the acquisition Signal-to-Noise-Ratio. Frequency domain simulations from the proposed model demonstrates that there is an optimum design point for all parameters involved in the building EOMOSFET pixel that allows to perform  $>9$  dB Signal-to-Noise-Ratio at  $<12 \mu\text{V}_{\text{RMS}}$  extracellular neuro-potentials power at the electrode node. This will finally enable high-resolution recording of ultra-weak neuro-potentials signals flowing by the electrolyte cleft that have not been never explored adopting planar capacitive coupling interfaces.

## 1 INTRODUCTION

There is a rather large lack of information between neuron membrane electrical activity of single neurons, and physiological or whole brain behavioural events. To fill this gap, we need to understand the activity of individual neurons and how it contributes to neural circuits functioning. Such ambitious perspective cannot be achieved by macroscale neural recording techniques (electroencephalogram, magnetic resonance, etc.), nor by patch clamps (monitoring single cell unit). One of the best options is to adopt Microelectrode-Arrays (MEAs, (Obien, 2015; Thomas, 1972; Pine, 1980)) that allow monitoring thousands of neurons/mm<sup>2</sup> by sensing: extracellular Action Potential (EAP in 300

Hz – 5 kHz bandwidth) and (in-vivo) Local Field Potential (LFP up to 300 Hz bandwidth). They are used as planar probes in neuron cells cultures forming a cell-electrode capacitive coupling. Implanted MEAs are typically needle-shaped probes that deeply penetrate the cortex for tissues recording/stimulating and for increasing proximity and signals detection rate.

Both in-culture and implantable MEAs can be integrated in commercial CMOS silicon substrates with an additional post-processing step consisting on covering CMOS metal aluminium electrodes by noble metal films (Pt/Au (Gross, 1982)) or dedicated oxide layers (TiO<sub>2</sub> (Cianci, 2012)). Active MEAs embed both analog signal processing channels (by neural amplifier, low-pass filter for antialiasing and A-to-D conversion) and digital circuits synthesizing

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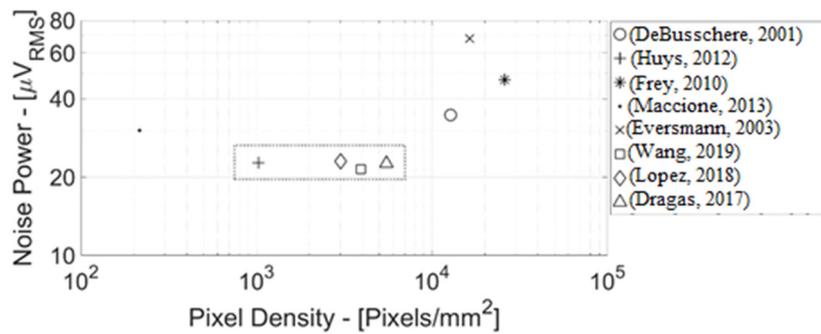


Figure 1: Microelectrode Arrays State-of-the-Art (Noise Power vs. Electrodes/Pixels Density).

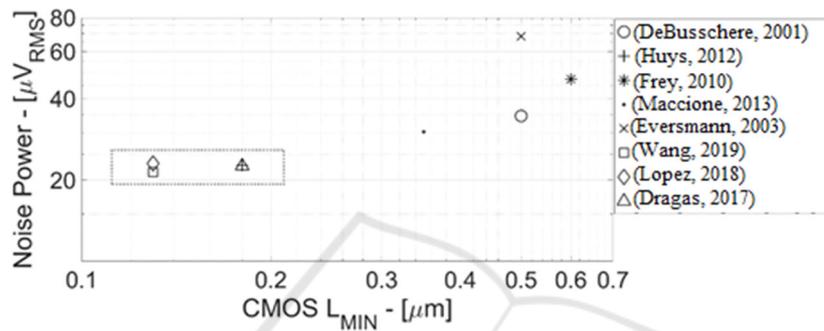


Figure 2: Microelectrode Arrays State-of-the-Art (Noise Power vs. CMOS Minimum Channel Length).

advanced Digital Spikes Detection ((Vallicelli, 2018; Shadid, 2009) DSD) algorithms. DSDs exploit the large array spatial resolution for separating relevant extracellular events from background noise by spatial correlation post-processing algorithms. They perform complex digital algorithm that require a certain computing power leading to a non-negligible dynamic power consumption and preventing integration in the same MEA silicon area.

Despite outstanding advancements in neural probes development, there are still many phenomena that state-of-the-art MEA technology cannot observe at high spatial resolution:

- at membrane level, subthreshold events, such as synaptic potentials can influence cell rest status without producing an action potential;
- propagation of the action potentials (AP) in axons, the backpropagation of AP in the dendrites and the generation of dendritic spikes, and weak extracellular synaptic field potential;
- traces of membrane oscillations in the extracellular space, never observed by planar probes since they require single-cell patch recording techniques.

Simply speaking, these events and phenomena cannot be observed because noise power floor in cell-electrolyte-electrode-electronics junction, is to date

higher than the signal power of those extracellular neuro-potentials carrying information coming from subthreshold or ultra-weak events.

Figure 1 shows some of most relevant MEAs state-of-the-art (DeBusschere, 2001; Huys, 2012; Frey, 2010; Maccione, 2013; Eversmann, 2003; Wang, 2019; Lopez, 2018; Dragas, 2017) in terms of noise power (in  $\mu V_{RMS}$  measured at the electrode node) vs. Pixel Density (electrodes count per  $mm^2$ ). Both axes are in log scale. There is a clear trend of noise power increasing with larger pixels density. Such trend is justified by the smaller electrode area (at higher pixel density) that increases flicker noise power coming from both the  $TiO_2$ /Metal film charge traps and the MOS transistor (MOST) placed just below the electrode.

In other words, to decrease the noise power and to detect sub-threshold events, it is necessary to increase the area of the single electrode but this would again lead to a reduction of the pixel density, degrading the neural recording spatial resolution.

Moreover, this approach has already reached the point of maximum efficiency because ref. (Huys, 2012; Dragas, 2017) in CMOS 0.18  $\mu m$  and ref. (Wang, 2019; Lopez, 2018) in CMOS 0.13  $\mu m$  (rectangular box in both Figure 1 and Figure 2) show practically the same noise power (i.e. approximately  $22 \mu V_{RMS}$ ) at the electrode equivalent node.

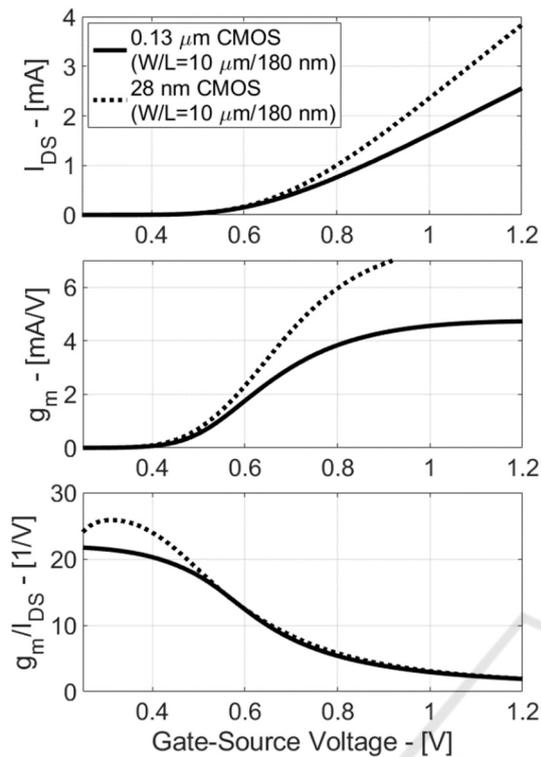


Figure 3: Drain-Source Current ( $I_{DS}$ ), Transconductance ( $g_m$ ) and Efficiency ( $g_m/I_{DS}$ ) in CMOS 0.18  $\mu\text{m}$  and 28 nm for Standard-Process MOST.

Furthermore, at such noise power levels, increasing electrode area (and thus reducing pixel density) does not involve a significant  $1/f$  (flicker) noise power reduction because MOS transistors thermal noise (in first approximation independent on electrode area and dependent on MOST dc current) becomes more dominant.

More specifically in-band thermal noise power spectral density is inversely proportional to the MOS transistor transconductance ( $g_m$ ). Such  $g_m$  is proportional to the current consumption, that (in bio-signals processing analog stages) operate the MOST with few  $\mu\text{A}$  current (Harrison, 2003). Thus the efficiency of the MOST (defined as  $g_m/I_{DS}$  ratio (Sansen, 2007) or in other words the amount of  $g_m$  that can be synthesized by a MOST operating at a certain drain-source current  $I_{DS}$ ) becomes a key parameter for both noise and power minimization in next generation MEAs.

Unfortunately, all most performant MEAs (Huys, 2012; Wang, 2019; Lopez, 2018; Dragas, 2017) are implemented in very old CMOS technologies (0.13  $\mu\text{m}$  processes nodes and beyond for flicker noise power reduction), where MOST efficiency is very much lower than nm-range CMOS nodes.

Figure 2 shows state-of-the-art MEAs noise power vs. CMOS process generation in terms of minimum MOST channel length.

Maximum (sub-threshold voltage) MOST efficiency in 0.13  $\mu\text{m}$  (or 0.18  $\mu\text{m}$  CMOS node) is about  $20 \text{ V}^{-1}$ , whereas 28 nm CMOS improves  $g_m/I_{DS}$  up to  $26 \text{ V}^{-1}$ , resulting in approximately +3dB electrode noise attenuation at same current.

These last considerations are validated in Figure 3, where MOST Drain-Source Current ( $I_{DS}$ ), Transconductance ( $g_m$ ) and Efficiency ( $g_m/I_{DS}$ ) are plotted vs. gate-source voltage in CMOS 0.13  $\mu\text{m}$  and 28 nm for Standard-Process MOSTs.

Moreover, older CMOS processes increases system complexity (Baschiroto, 2009; De Matteis, 2006) and harness, because Digital Spikes Detection stages cannot be on-chip integrated due to its very high dynamic power in low scaled-down CMOS nodes. Effectively such power will be incompatible with a stable spatial temperature distribution for cell integrity in neuron cultures and with the limited power budget required by the portability of implantable devices.

In this context, this paper proposes a dedicated design of EOMOSFET MEAs (for the case of a single recording site/pixel and that can be easily extended to spatial matrix MEAs) that efficiently sets the basis for definitely overcome the above issues by:

- adopting the CMOS 28 nm technology node and then including in the model the technology node parameters like dielectric constant, gate capacitance per unit area, sub-threshold slope factor coefficient, etc. This enables two key improvements:
  - to take advantage of the higher  $g_m$  (and lower thermal noise power spectral density) for a given current of analog CMOS 28 nm SP MOST against 0.13  $\mu\text{m}$  and beyond;
  - to use on-chip DSD stages without exceeding in extra-power (by ultra-low digital dynamic power for Standard-Process MOST);
- rejecting the flicker noise by maintaining the electrode area equal to  $100 \mu\text{m}^2$  (approximately three times lower than neuron area) enabling about 1 k neuron recording for  $1 \text{ mm}^2$  active MEA area.

This paper is organized as follows. Section 2 describes the cross-section layers of the CMOS 28 nm EOMOSFET pixel and all relevant signal/noise transfer functions as a function of the interface electrical parameters. Section 3 presents the

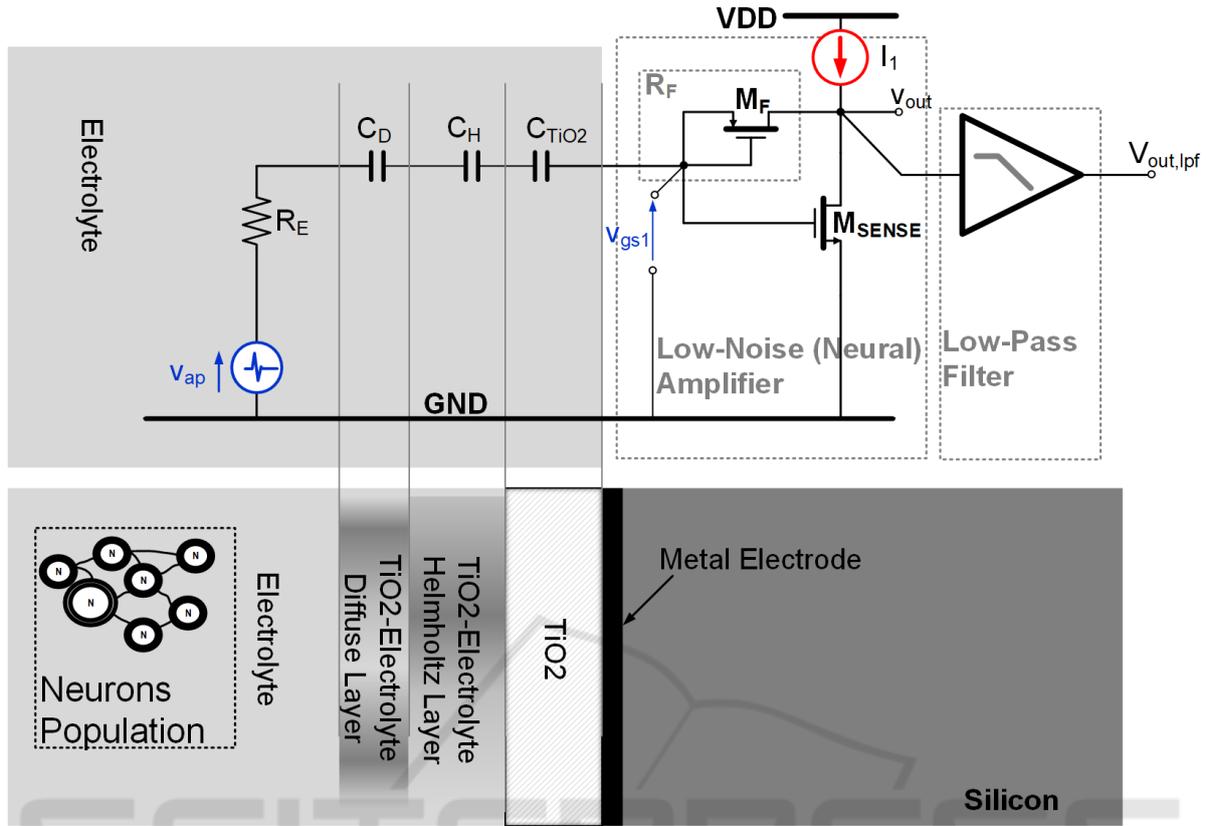


Figure 4: EOMOSFET Single Pixel Cross-Section.

simulation results of the model and the selected design point that allows to perform >9 dB SNR with < 12  $\mu V_{RMS}$  neuro-potentials signals power. At the end of the paper conclusions will be drawn.

## 2 EOMOSFET CROSS-SECTION AND ELECTRICAL CHARACTERISTICS

EOMOSFET biosensors are spatially organized in a matrix of pixels. The proposed model is based on the the single pixel electrical scheme shown in Figure 4. The neuron population and the silicon die separated by an electrolyte bath (NaCL at 0.1 Moles concentration). The  $TiO_2$  post-processing layer (Cianci, 2012) isolates the silicon circuits from the biological environment. The extracellular ionic currents flow by the electrolyte equivalent resistance ( $R_E$ ) inducing a small voltage variation. Thus, the voltage across  $R_E$  is coupled with the  $TiO_2$  capacitance ( $C_{TiO2}$ ) by the  $C_D$ - $C_H$  series, where  $C_D$  and  $C_H$  are the double-layer region capacitances (Diffuse and Helmholtz layers capacitances, respectively

(Massobrio, 2016)). Just beneath the  $TiO_2$  there is an on-chip metal electrode, whose area ( $A_{ELE}$ ) is in this case  $100 \mu m^2$  (here  $M_{SENSE}$  area is 50% lower to maintain the imaging resolution). This oxide layer has approximately 6 nm thickness and builds a specific series capacitance ( $C_{TiO2}$ ).

Notice that this scheme is referred to the worst case scenario of scarce neuron-chip adhesion (Massobrio, 2016), where neuro-potentials signals are very weak and are spread across the electrolyte bath. Thus the voltage source ( $v_{in}$ ) models both EAP and LFP signals.

Thus, the equivalent capacitance ( $C_{HDT}$ ) between the cells and the MOS transistor (MOST)  $M_{SENSE}$  gate is given by eq. (1):

$$C_{HDT} = \frac{1}{1/C_D + 1/C_H + 1/C_T} \quad (1)$$

$C_D$  and  $C_H$  capacitances depend on the charge concentration at the electrolyte-oxide interface.

More specifically such Helmholtz and diffuse layers capacitances can be calculated using the metal electrode area ( $A_{ELE}$ ), the water permittivity ( $\epsilon_w = 78.4 \cdot \epsilon_0$  where  $\epsilon_0$  is the vacuum permittivity equal to 8.85 pF/m) and two physical lengths  $L_D$  (Deybe

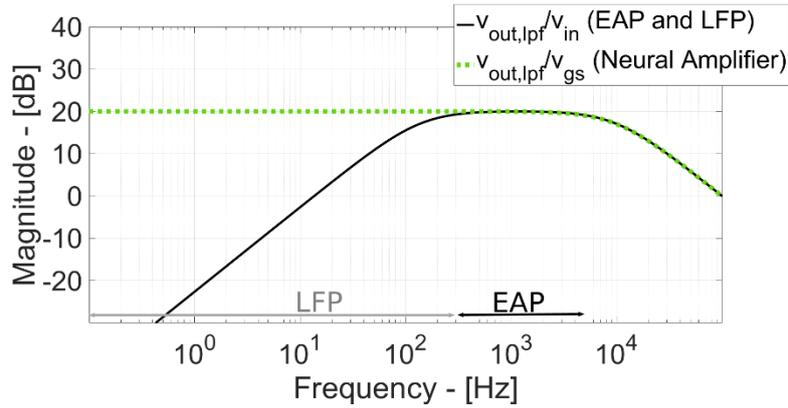


Figure 5: Signal Frequency Response.

Table 1: Neuron-Silicon Electrical Model Parameters.

Parameter	Explanation	Value
$A_{ELE}$	Metal Electrode Area	$100 \mu\text{m}^2$
$R_E$	Electrolyte Bulk Resistance	$125 \text{ k}\Omega$
$C_D$	Stern Capacitance	$35.9 \text{ pF}$
$C_H$	Helmutz Capacitance	$17.3 \text{ pF}$
$C_T$	TiO2 Capacitance	$3.3 \text{ pF}$
$M_{SENSE}$ $W_S/L_S$	$M_{SENSE}$ Aspect Ratio	$50 \mu\text{m} / 1 \mu\text{m}$
$g_{ms}$	$M_{SENSE}$ Transconductance	$50 \mu\text{A/V}$
$r_{ds}$	$M_{SENSE}$ Output Resistance	$187 \text{ k}\Omega$
$\tau_{LP}$	Low-Pass Filter Dominant Time-Constant	$100 \mu\text{s}$ (10 kHz)
$R_F$	Pseudo-Resistor Value	$5 \text{ G}\Omega$

length, equal to 1 nm) and  $x_2$  (Stern length, equal to 2 nm) depending on the electrolyte-oxide interface (Massobrio, 2016).

$$C_D = \frac{\epsilon_w}{L_D} \cdot A_{ELE} \quad \text{and} \quad C_H = \frac{\epsilon_w}{x_2} \cdot A_{ELE} \quad (2)$$

The  $\text{TiO}_2$  isolation layer capacitance has  $45 \cdot \epsilon_0$  and 6 nm permittivity and thickness, respectively (Cianci, 2012):

$$C_T = \frac{\epsilon_{\text{TiO}_2}}{x_{\text{TiO}_2}} \cdot A_{ELE} \quad (3)$$

Table 1 resumes the main values of the neuron-electronics junction electrical model.

Hence, the  $M_{SENSE}$  MOST is the core of a dedicated neural Low-Noise-Amplifier (LNA) that drives an ideal low-pass filter whose main aim is to limit the signal bandwidth at 10 kHz.  $M_{SENSE}$  small-signal current is proportional (by its transconductance ( $g_{ms}$ )) to the induced extracellular AP and LFP ( $v_{in}$ ). The  $M_{SENSE}$  MOST is here biased by a feedback pseudo-resistor ( $M_F$ ) to synthesize a very high resistance ( $R_F$  in the order of few  $\text{G}\Omega$ ) that sets the low frequency pole (where LNA bandwidth starts).

The electrolyte bulk plays a key role for both signal and noise transfer function. Its equivalent resistance  $R_E$  depends on the electrolyte bulk conductivity  $k'$  and on the metal electrode area  $A_{ELE}$  (Deen, 2006) as follows:

$$R_E = \frac{1}{k'} \cdot \sqrt{\pi/A_{ELE}} \quad (4)$$

Assuming the same number of carriers ( $N_C=N_P=N_N$ ) for both positive ( $N_P$ , cations) and negative ( $N_N$ , anions) charges, then the bulk electrolyte conductivity is related with the moles concentration ( $N_{MOL}$ ) and the water density ( $\rho=1000 \text{ Kg/m}^3$ ) as expressed in eq. 5 (Park, 2016):

$$k' = q \cdot (\mu_P \cdot N_P + \mu_N \cdot N_N) = q \cdot (\mu_P + \mu_N) \cdot N_C = q \cdot (\mu_P + \mu_N) \cdot \rho \cdot N_{MOL} \quad (5)$$

where  $\mu_P$ - $\mu_N$  are the mobility coefficients for cations-anions, respectively. Thus, the bulk electrolyte conductivity is equal to  $12.6 \text{ mA}/(\text{V}\cdot\text{m})$  and the bulk resistance  $R_E$  is then  $125 \text{ k}\Omega$  at  $100 \text{ mM}$ .

## 2.1 EAP and LFP Signal Transfer Function

Previous considerations definitively fix the numerical values of all parameters involved in neuron-electronics junction as a function of the physical size and characteristics of the several layers composing the EOMOSFET pixel. It is thus possible to calculate the small signal transfer function for all relevant signal and noise contributions. This will provide a frequency domain map of the achievable Signal-to-Noise-Ratio and, more importantly, a clear limit in terms of maximum allowable noise power for analog stages with the main aim to avoid significant SNR degradation.

Input signal  $v_{in}$  includes both EAP and LFP neuro-potentials. The transfer function between input signal

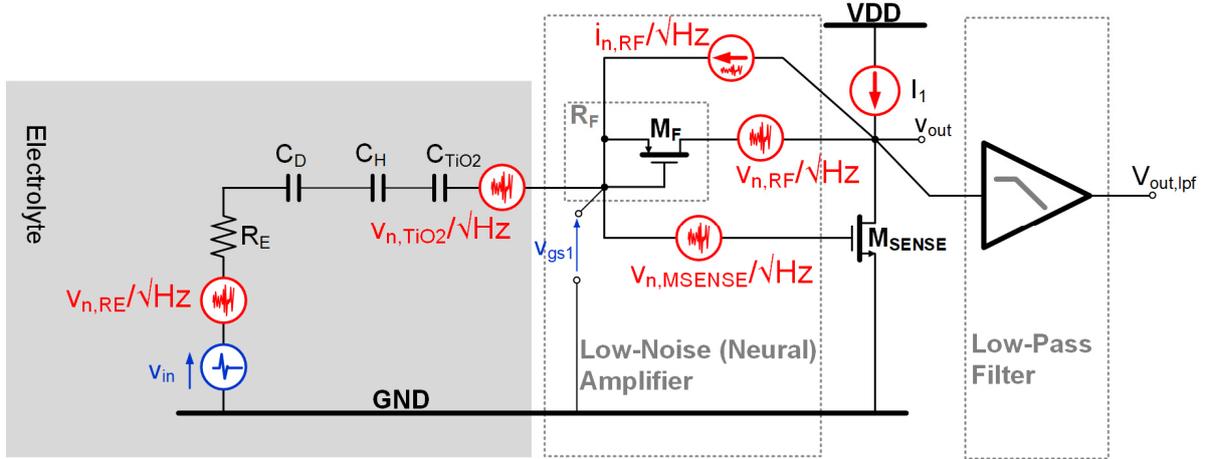


Figure 6: Noise Sources Frequency Response.

( $v_{in}$ ) and Low-Pass Filter (LPF) output node ( $v_{out,lpf}/v_{in}$  in Laplace domain) is given by eq. 6:

$$\frac{v_{out,lpf}}{v_{in}}(s) = \frac{g_{ms} \cdot r_{ds}}{1 + g_{ms} \cdot r_{ds}} \cdot \frac{s \cdot C_{HDT} \cdot R_F}{1 + s \cdot \frac{C_{HDT} \cdot R_F}{g_{ms} \cdot r_{ds}}} \cdot \frac{1}{1 + s \cdot \tau_{LP}} \quad (6)$$

where  $g_{ms}$  and  $r_{ds}$  are  $M_{SENSE}$  MOST small-signal parameters, and  $\tau_{LP}$  is the low-pass filter dominant time constant (fixing the LPF -3dB passband at 10 kHz). Figure 5 shows the corresponding eq. 6 frequency response and includes the analog signal processing (Neural Amplifier and Low-Pass Filter) frequency response. Thanks to the very high resistance synthesized by pseudo-resistors (5 G $\Omega$ ), the dominant pole time constant ( $C_{HDT} \cdot R_F / (g_{ms} \cdot r_{ds})$ ) has a frequency of 136 Hz and more importantly the gain is higher than 0 dB (i.e.) from 13 Hz (channel starts to amplify the input signal) enabling recording of ultra-weak slow-oscillation and/or low-frequency neuro-potentials.

## 2.2 Noise Transfer Function

Figure 6 shows the EOMOSFET pixel equivalent circuit with the most relevant noise sources (coming from electrolyte resistance  $R_E$  ( $v_{n,RE}$ ),  $TiO_2$  film ( $v_{n,TiO2}$ ), feedback pseudo-resistor  $R_F$  ( $v_{n,RF}$ ) and sensing MOST  $M_{SENSE}$  ( $v_{n,MSENSE}$ )). The analog front-end is composed by the cascade of a neutral Low-Noise-Amplifier (LNA, for neural signal read-out and amplification) driving a Low-Pass Filter (LPF) at 10 kHz -3dB bandwidth for signal selection and out-of-band noise rejection. The amount of noise at the output of the analog signal processing chain ( $v_{out,lpf}$ , i.e. the LPF output node) depends on the specific noise power of each noise source and the frequency response associated to each noise source.

### 2.2.1 $R_E$ Thermal Noise

The electrolyte resistance ( $R_E$ ) generates thermal noise ( $v_{n,RE}$ ) whose in-band power spectral density is given by eq. 7:

$$\frac{\langle v_{n,RE}^2 \rangle}{\Delta f} = 4 \cdot k \cdot T \cdot R_E \quad (7)$$

$k$  and  $T$  are Boltzman constant and temperature (300 K) and  $R_E$  is 125 k $\Omega$  as reported in eq.4 and Table 1. The  $v_{out}/v_{n,RE}$  transfer function (in Laplace domain) gives the total amount of voltage signal at the output of the filter as a function of  $C_{HDT}$  capacitance ( $C_H$ ,  $C_D$ , and  $C_{TiO2}$  serie), the feedback pseudo-resistor ( $R_F$ ) and  $M_{SENSE}$  MOST main small-signal parameters (transconductance ( $g_{ms}$ ) and output resistance ( $r_{ds}$ )):

$$\frac{v_{out,lpf}}{v_{n,RE}}(s) = \frac{g_{ms} \cdot r_{ds}}{1 + g_{ms} \cdot r_{ds}} \cdot \frac{s \cdot C_{HDT} \cdot R_F}{1 + s \cdot \frac{C_{HDT} \cdot R_F}{g_{ms} \cdot r_{ds}}} \cdot \frac{1}{1 + s \cdot \tau_{LP}} \quad (8)$$

Figure 7 illustrates the corresponding frequency response and demonstrates that  $R_E$  thermal noise has the same signal transfer function. This is even demonstrated by Figure 8 where the noise power spectral density (PSD) for every EOMOSFET noise source with the total noise PSD is plotted.

Effectively  $R_E$  noise PSD (green line) perfectly overlap the  $v_{in}$  signal bandwidth and thus it is one of the most relevant ineliminable noise sources in EOMOSFET pixels and more generally in planar capacitively-coupled neural probes/MEAs.

### 2.2.2 $TiO_2$ Flicker Noise

$TiO_2$  film (used to separate or couple the biological environment from silicon chip) mainly generates

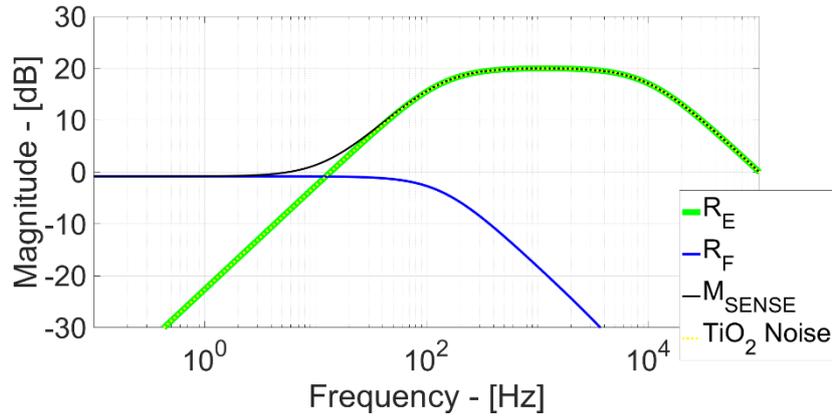


Figure 7: Noise Sources Frequency Response.

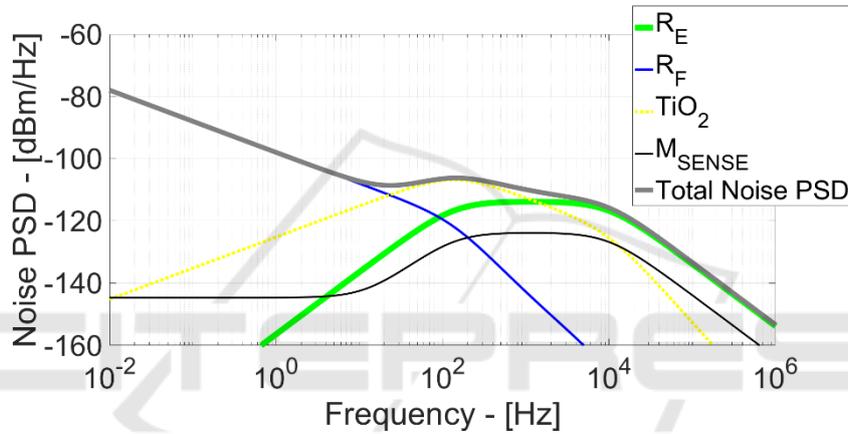


Figure 8: Output Noise PSD.

flicker noise. Its power source is inversely proportional to the frequency  $f$ , as follows:

$$\frac{\langle v_{n,TiO_2}^2 \rangle}{\Delta f} = \frac{k_{pf,TiO_2}}{C_{TiO_2}} \cdot \frac{1}{f} \quad (9)$$

where  $k_{pf,TiO_2}$  is the specific flicker constant and  $C_{TiO_2}$  is the equivalent  $TiO_2$  capacitance.  $v_{n,TiO_2}$  has the same transfer function as  $v_{n,RE}$  (eq. 8). In this model  $TiO_2$  has been preferred to other neuron-silicon junction coupling options, because it has lower flicker noise power comparing with Pt/Au noble metal films that can exhibit an  $1/f^2$  noise, increasing the low frequency noise power at the output of the neural amplifier.

Nonetheless the intrinsic neuron-electronics junction ac-coupling allows some filtering of  $TiO_2$  flicker at low frequency. Afterwards, starting from 136 Hz,  $v_{n,TiO_2}$  frequency response has 20 dB gain but, at the same time,  $TiO_2$   $1/f$  noise behaviour has already reduced its noise power. This generate a  $TiO_2$  noise PSD maximum at 132 Hz and, after this frequency, the circuit attenuates the  $TiO_2$  flicker noise power.

### 2.2.3 $M_{SENSE}$ Noise

The main noise contributions of the neural amplifier come from  $M_{SENSE}$  and  $R_F$  (feedback pseudo-resistor).  $M_{SENSE}$  is a MOST biased in subthreshold region synthesizing  $50 \mu A/V$  transconductance  $g_{ms}$ . This value allows to minimize  $M_{SENSE}$  thermal noise at few  $\mu A$  current consumption and thus making feasible the integration of the proposed EOMOSFET setup in thousands of pixels resolution spatial grid/matrix without excess of power. The equivalent model for  $M_{SENSE}$  noise source is:

$$\frac{\langle v_{n,MSENSE}^2 \rangle}{\Delta f} = \frac{k_F}{W_S \cdot L_S} \cdot \frac{1}{f} + \frac{2}{3} \cdot 4 \cdot k \cdot T \cdot \frac{1}{g_{ms}} \quad (10)$$

where  $k_F$  is the CMOS 28 nm flicker constant and  $W_S$  and  $L_S$  are  $M_{SENSE}$  width and length. The transfer function associated to the  $v_{n,MSENSE}$  noise source is:

$$\frac{v_{out,lpf}}{v_{n,MSENSE}}(s) \cong \frac{g_{ms} \cdot r_{ds}}{1 + g_{ms} \cdot r_{ds}} \cdot \frac{1 + s \cdot C_{HDT} \cdot R_F}{1 + s \cdot \frac{C_{HDT} \cdot R_F}{g_{ms} \cdot r_{ds}}} \cdot \frac{1}{1 + s \cdot \tau_{LP}} \quad (11)$$

At low frequency ( $\ll 13$  Hz) the  $C_{HDT}$  capacitor behaves like an open circuit.  $M_{SENSE}$  is then diode-connected and thus its noise source transfers to the output by unitary gain. At very high frequency ( $\gg 13$  Hz)  $C_{HDT}$  features very low impedance (ideally a short circuit), then the feedback is broken and  $v_{n,MSENSE}$  is directly applied between  $M_{SENSE}$  gate and ground. Thus output voltage noise is 20 dB higher. One of the objectives of this model is to minimize such noise contribution by acting on both  $M_{SENSE}$  area ( $W \cdot L$  for flicker noise power reduction, here set at  $50 \mu\text{m}^2$ ) and transconductance (for thermal noise power reduction at  $50 \mu\text{A/V}$  resulting in  $14.8 \text{ nV}/\sqrt{\text{Hz}}$  in-band noise PSD).

### 2.2.4 $R_F$ Pseudo-resistor Noise

To enhance the pass-band gain of the EOMOSFET pixel and to enable observation of ultra-weak ultra-low frequency neuro-potential signals, the feedback resistance must be in the  $G\Omega$  order. Integrated resistors in silicon technologies are not a feasible option for such a large resistance value, hence this model adopts a MOST in off region (pseudo-resistor) where gate-source nodes are shorted, preventing any conductive channel between drain and source and exploiting the parasitic diodes formed by source-bulk and drain-bulk junctions. Such diodes are automatically biased in reverse region synthesising a very high resistance ( $5 G\Omega$  in this case). Starting from these considerations, the  $R_F$  pseudo-resistor noise source has two main noise sources: shot (from diodes) and flicker as follows:

$$\frac{\langle v_{n,RF}^2 \rangle}{\Delta f} = \frac{k_F}{W_F \cdot L_F} \cdot \frac{1}{f} \quad (12)$$

$$\frac{\langle i_{n,RF}^2 \rangle}{\Delta f} = 2 \cdot q \cdot I_{LEAK} \quad (13)$$

where  $W_F$  and  $L_F$  are width and length of the pseudo-resistor MOST,  $I_{LEAK}$  is the leakage current mainly coming from  $M_{SENSE}$  gate oxide and approximately equal to few pA. Notice that since  $R_F$  is connected in feedback, its noise is relevant at very low frequency ( $< 136$  Hz). So, this effect will be important in  $13 \text{ Hz} - 136 \text{ Hz}$  bandwidth. The transfer functions for  $v_{n,RF}$  and  $i_{n,RF}$  noise sources are respectively:

$$\frac{v_{out,lpf}}{v_{n,RF}}(s) \cong \frac{g_{ms} \tau_{ds}}{1 + g_{ms} \tau_{ds}} \cdot \frac{1 + s \cdot C_{HDT} \cdot R_E}{1 + s \cdot \frac{C_{HDT} \cdot R_F}{g_{ms} \tau_{ds}}} \cdot \frac{1}{1 + s \cdot \tau_{LP}} \quad (14)$$

$$\frac{v_{out,lpf}}{i_{n,RF}}(s) \cong R_F \cdot \frac{g_{ms} \tau_{ds}}{1 + g_{ms} \tau_{ds}} \cdot \frac{1 + s \cdot C_{HDT} \cdot R_E}{1 + s \cdot \frac{C_{HDT} \cdot R_F}{g_{ms} \tau_{ds}}} \cdot \frac{1}{1 + s \cdot \tau_{LP}} \quad (15)$$

Table 2: Noise Summary.

Bandwidth	Noise Source	Value [ $\mu\text{VRMS}$ ]
< 300 Hz	$R_E$	5.5
	$\text{TiO}_2$	15.7
	$R_F$	10.4
	$M_{SENSE}$	1.73
	<b>Total Noise</b>	<b>19</b>
300 Hz – 5 kHz	$R_E$	30
	$\text{TiO}_2$	27.2
	$R_F$	1
	$M_{SENSE}$	9.5
	<b>Total Noise</b>	<b>42</b>
< 5 kHz	$R_E$	30.6
	$\text{TiO}_2$	31.4
	$R_F$	10.4
	$M_{SENSE}$	9.66
	<b>Total Noise</b>	<b>46.08</b>

## 3 NOISE SUMMARY AND SIGNAL-TO-NOISE-RATIO

The small-signal electrical and analytical model based on Figure 6 scheme allow to easily evaluate the noise and signal behaviour across the EOMOSFET pixel.

More in details, by reducing the  $M_{SENSE}$  MOST thermal/flicker noise power and taking into account both shot and flicker noise sources coming from MF pseudo-resistor, the presented setup enables very low noise performances ( $1.9 \mu\text{VRMS}$  and  $4.2 \mu\text{VRMS}$ ) at the electrode (or at the  $M_{SENSE}$  gate node).

Table 2 presents the noise summary of this specific setup where, in both LFP and EAP bandwidths, dominant noise contributions come from electrolyte bath (thermal) and  $\text{TiO}_2$  (flicker) coupling.

In other words by a dedicated design of the interface in terms of both biological and circuital electrical parameters, it is possible to set MOSTs ( $M_{SENSE}$  and  $M_F$ ) dc current and aspect ratio with the main aim to minimize read-out noise power and in first approximation remaining with the only interface noise due to the electrolyte-electrode junction.

Effectively in LFP bandwidth, total noise (measured at the low-pass filter output node) is  $19 \mu\text{VRMS}$  (with  $5.5 \mu\text{VRMS}$   $R_E$  noise power and  $15.7 \mu\text{VRMS}$   $\text{TiO}_2$  noise power, respectively).

In EAP bandwidth, total output noise is  $42 \mu\text{VRMS}$  when  $R_E$  and  $\text{TiO}_2$  have  $30 \mu\text{VRMS}$  and  $27.2 \mu\text{VRMS}$  noise power, respectively.

About SNR performances, Table 3 reports a final resume of the achieved SNR in both EAP and LFP bandwidths, also including Noise Figure performances.

Table 3: Noise Summary, SNR and Noise Figure.

Parameter	Explanation	Value
< 300 Hz Output Noise	LFP Bandwidth Output Noise	19 $\mu\text{V}_{\text{RMS}}$
< 300 Hz Electrolyte Noise	LFP Bandwidth $\text{TiO}_2+\text{R}_E$ Output Noise	16.63 $\mu\text{V}_{\text{RMS}}$
< 300 Hz Electrode SNR at $v_{\text{in}}=10 \mu\text{V}_{\text{RMS}}$	LFP Bandwidth SNR at the Electrode (considering only $\text{TiO}_2$ and $\text{R}_E$ Noise)	15.5 dB
< 300 Hz LPF SNR	LFP Bandwidth Output SNR (at the LPF Output Node)	14.42dB
< 300 Hz NF	LFP Noise Figure	1.15 dB
300 Hz - 5 kHz Output Noise	EAP Bandwidth Output Noise	42 $\mu\text{V}_{\text{RMS}}$
300 Hz - 5 kHz Electrolyte Noise	EAP Bandwidth $\text{TiO}_2+\text{R}_E$ Output Noise	40.5 $\mu\text{V}_{\text{RMS}}$
300 Hz - 5 kHz Electrode SNR at $v_{\text{in}}=10 \mu\text{V}_{\text{RMS}}$	EAP Bandwidth SNR at the Electrode (considering only $\text{TiO}_2$ and $\text{R}_E$ Noise)	7.8 dB
300 Hz - 5 kHz LPF SNR	EAP Bandwidth Output SNR (at the LPF Output Node)	7.5 dB
300 Hz - 5 kHz NF	EAP Noise Figure	0.31 dB

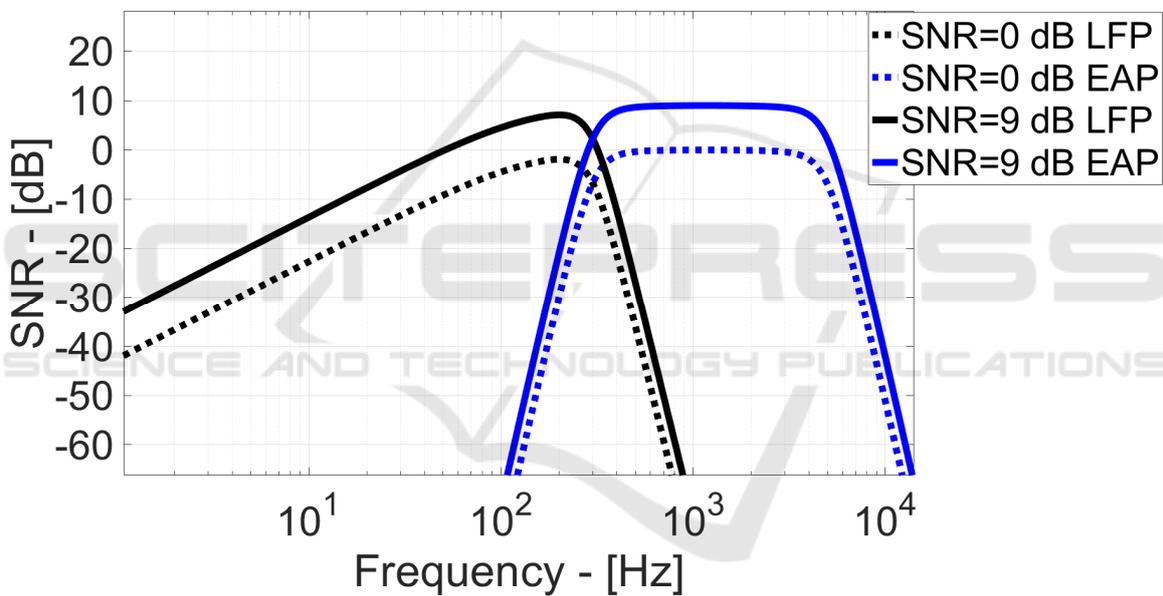


Figure 9: SNR vs. Frequency for LFP and EAP.

Assuming  $10 \mu\text{V}_{\text{RMS}}$  LFP signal at electrolyte bath level (state-of-the-art (DeBusschere, 2001; Huys, 2012; Frey, 2010; Maccione, 2013; Eversmann, 2003; Wang, 2019; Lopez, 2018; Dragas, 2017) operates with  $>22 \mu\text{V}_{\text{RMS}}$  detection threshold), the SNR at the electrode (without considering the LNA additional noise) is 15.5 dB and after amplification 14.42, resulting in very low noise figure of 1.15 dB. More interestingly, since most of DSD detects neuro-potential spikes with  $\text{SNR} \geq 9 \text{ dB}$  (Shahid, 2009), then the proposed EOMOSFET setup enables the detection of  $< 10 \mu\text{V}_{\text{RMS}}$  slow ultra-weak events.

At  $10 \mu\text{V}_{\text{RMS}}$  EAP, Noise Figure is 0.31 dB, meaning that the system introduces a very negligible degradation of the SNR.

Finally, Figure 9 shows the SNR vs. frequency when LFP/EAP input signal power equals the noise power in the corresponding bandwidths (0 dB SNR) and when such signal power is 9 dB higher than the noise.

Effectively, the proposed analog read-out has a certain frequency-dependent channel response (mainly due to the  $R_F$  low frequency bandwidth limitations). Thus, some neuro-potential signals can experience different gain values and, at the same noise power, this results in different SNR.

Maximum 7.5dB SNR is achieved at 201 Hz with 5.5  $\mu\text{V}_{\text{RMS}}$  LFP signal power. For EAP neuro-potentials, SNR reaches 9 dB with 11.8  $\mu\text{V}_{\text{RMS}}$  input power, against 22  $\mu\text{V}_{\text{RMS}}$  state-of-the-art in Figure 1 and Figure 2.

Hence, this demonstrates that the presented setup can be adopted for thousands of pixels resolution MEAs with the key advantage of improving the noise performances and thus decreasing the minimum detectable signals power.

## 4 CONCLUSIONS

In this paper a complete electrical model of a single-pixel Electrolyte-Oxide MOS Field-Effect-Transistors neural interface has been presented. The model includes all biological and electrical parameters building the interface. Thanks to specific noise and signal simulation results, the proposed setup allows optimum design and sizing of all MOS transistors embedded in the analog signal processing, minimizing noise power, and enabling ultra-weak slow oscillation detection. More specifically the proposed optimum design features 9 dB SNR at 11.8  $\mu\text{V}_{\text{RMS}}$  extra-cellular Action Potentials power and 7.8 dB SNR for 5.5  $\mu\text{V}_{\text{RMS}}$  Local Field Potentials, at the electrode node.

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