Current Loop Stability Analysis of a VIENNA-type Three-phase Rectifier for an Imaging System Power Supply Application

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Abstract: High power supply for imaging systems needs to meet increasing demand in speed, power and voltage control. A Vienna-type three-phase rectifier prototype has been developed by GE Healthcare to handle it. This power supply has a significant stability issue because its load has a pulsed profile, and the ranges of power demand, input voltage, and grid impedance are wide. First, a model of the rectifier and its control has been made. Second, a current loop stability analysis has been investigated. Stability margins have been drawn for all the range of output power, input voltage and grid inductance for the current loop. Stability has been shown for all the operating points. However, a poorly damped input filter brings potential oscillations and reduces stability margins. Delay margins are also particularly low. Finally, a validation of the rectifier model has been made with measurements on the prototype.

1 INTRODUCTION

High-power imaging systems (MRI, X-ray scanner,etc...) are powered from the Hospital power grid through a multi-converters which has the following functions :

- An AC/DC conversion to provide a DC voltage for main load (X-Ray Generators) ;
- An isolation from grid;
- A DC/AC conversion to provide an AC three-phase voltage for auxiliary loads;

The AC/DC Converter has to handle large constraints:

- Step power from a few kilowatts to a hundreds kilowatts from main load;
- Transparent mode operation despite a wide range of nominal input voltage and input grid impedance.

In order to improve image quality, these systems need accurate dc voltage regulation to increase the power and speed for capturing images.

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There are also additional industrial constraints on cost and volume which must be taken into account when designing a new power supply.

Until now, the AC/DC converter is a passive three-phase rectifier. And the low-frequency three-phase transformer which provides the isolation has a big volume. Consequently the output DC voltage is unregulated, the power supply has a low efficiency and a large volume, although its cost is low. Thus it limits the available peak power and the slope of pulsed load.

Active three-phase unidirectional rectifier addresses output voltage regulation, high efficiency, low volume. It enables also the use of a smaller high frequency transformer. Among the active rectifier, the Vienna topology has a regulated output, good reliability, good power density, a low total harmonic distortion and is well documented (Leibl, 2017) (Kolar and Friedli, 2011). A prototype of an modified Vienna (cf. Fig. 3) has been successfully built by GE Healthcare and validated for several operating points.

In order to validate this topology and its control strategy, this paper investigates the stability margins on a wider range of operating points. The control model of Vienna (cf. Fig. 5) is made of three control loops on input currents, total output voltage and output midpoint voltage. The main stability issues ap-

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pears in the input currents control loop because it is the fastest loop. Consequently only the current loop will be studied. A single variable approach has been chosen to clearly highlight the main issues regarding resonances and stability margins.

The paper is organized as followed. Section 2 describes a model of the modified Vienna Rectifier and its control strategy. Section 3 draws the stability margins of the current loop over one phase from a linearised averaged model. A sweep of output power, input nominal voltage and grid inductance shows the weakest operating points. Section 4 shows a validation of the model by comparison with measurements of the total output voltage and of one input current under a power load step. Section 5 concludes the main finding of this paper and discusses future work.

2 RECTIFIER MODELLING AND CONTROL

Fig. 1 shows how the power is supplied to the imaging system. A transformer makes a connection between power grid and hospital's grid. It limits the available power to 150kVA.

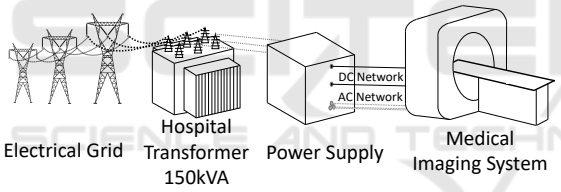

Figure 1: Power transmission chain between power grid and medical imaging systems.

Load profile is shown in Fig. 2. Power supply must face with low average power and high peak power.

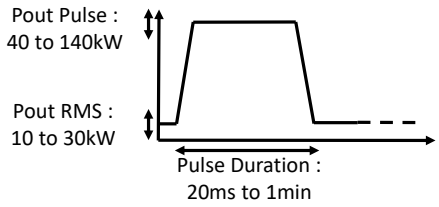

Figure 2: Load profile seen by power supply of a x-ray scanner.

2.1 Rectifier Topology

Rectifier topology (cf. Fig.3) is composed by two interleaved Vienna (Kolar and Friedli, 2011) and coupled boost inductances for each phase. This is why it has been named Coupled-Inductances Interleaved Vienna Rectifier (C2IV Rectifier).

A two parallel converters topology has been chosen to divide current constraints on semiconductors by two.

The input phase voltages V_a, V_b and V_c are ideal three-phase voltage source. The grid line between phase voltages and C2IV is modelled by an inductance L_g in series with a resistance R_g.

The input filter is composed by three capacitors C_x in star connection with their parasitic resistors R_x in series. The artificial neutral point of this filter is connected to the ouptut midpoint voltage M for common mode filtering.

Boost Inductances L of phase 1 and 2 are coupled. (COSTAN, 2007) shows the advantages of inductances coupling. Combined with an interleaved command of the two phase of the converters, current ripples in grid and in inductances see their amplitude divided by two and their frequency multiplied by two. Consequently, inductance size can be reduced for the same constraints in current ripple.

The chosen bidirectional switch is a T-type bridge-leg structure (cf. Fig.4) with two IGBT and two antiparallel diodes. Its main advantage is low cost because of its usage for three-phase inverters.

Table 1 shows the value of hardware parameters of the C2IV prototype.

Table 1: Simulation Parameters.

Invariant Parameters	Units	Value	
Output DC voltage V_{dc}	V	800	
Output capacitors C	µF	4240	
Boost inductance L	µH	800	
Boost mutual M	µH	760	
Intern resistance R_l	mΩ	100	
Input capacitors C_x	µF	10	
Parasitic resistance Rx	mΩ	3	
Grid frequency f_{grid}	Hz	50	
Switching frequency f_{sw}	kHz	23	
Variable Parameters	**Units**	**Min**	**Max**
Ouptut power P_{out}	kW	10	140
Input AC voltage V_{in}	V_{llrms}	342	528
Grid inductance L_g	µH	10	300
Grid resistance R_g	mΩ	10	120

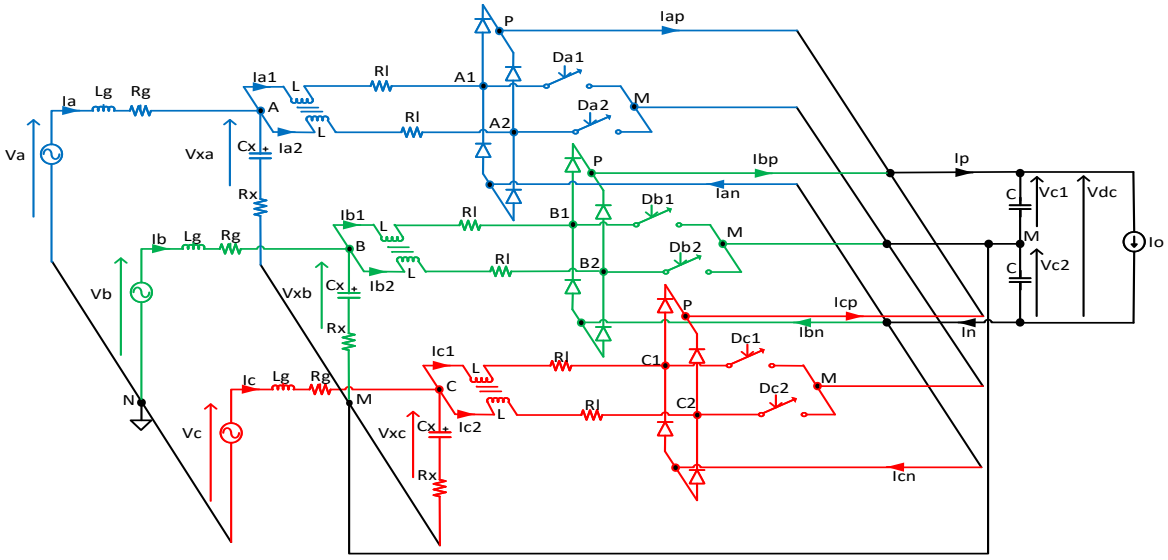

Figure 3: Schematic of the Coupled-Inductances Interleaved-Vienna Rectifier (C2IV) in a pseudo-3D view.

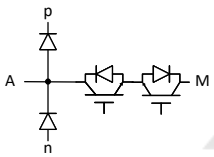

Figure 4: T-Type bridge-leg structure.

2.2 Rectifier Modelling

Assumptions made to obtain state space equations are identical to what has already been done for Vienna rectifier in (Lai et al., 2009) and will not be detailed.

Every identical variables (currents, voltages, switch commands) are put together in vectors to simplify the writing of differential equations.

For each inductance and each capacitor corresponds a state variable as seen in Fig. 3. There are 14 state variables.

Input currents in boost inductances L are shown in eq.1 :

$$I_{abc12} = (I_{a1} \quad I_{b1} \quad I_{c1} \quad I_{a2} \quad I_{b2} \quad I_{c2}) \tag{1}$$

Output voltages across the output capacitances C are shown in eq.2 :

$$V_{c12} = (V_{c1} \quad V_{c2}) \tag{2}$$

Phase currents in grid inductances L_g are shown in eq.3 :

$$I_{abc} = (I_a \quad I_b \quad I_c) \tag{3}$$

Input filter voltages across capacitances C_x are shown in eq.4:

$$V_{xabc} = (V_{xa} \quad V_{xb} \quad V_{xc}) \tag{4}$$

There are 6 control variables shown in eq.5, because each bidirectional switch is controlled by only one signal :

$$D_{abc12} = (D_{a1} \quad D_{b1} \quad D_{c1} \quad D_{a2} \quad D_{b2} \quad D_{c2}) \tag{5}$$

In real-time equations, D_{abc12} stands for the switching states which take the value 0 or 1. In average equations,D_{abc12} stands for the duty-cycles .

Perturbation variables are the three phase voltages (cf. eq.6) and the output current (cf. eq.7) :

$$V_{abc} = (V_a \quad V_b \quad V_c) \tag{6}$$

$$I_{out} = (I_o \quad I_o) \tag{7}$$

Matrices of coupling inductances (cf. eq.8), of duty-cycles (cf. eq.9) and of input currents sign (cf. eq.10) are used to further simplify writings of differential equations.

$$[L \quad M] = \begin{pmatrix} L & 0 & 0 & M & 0 & 0 \\ 0 & L & 0 & 0 & M & 0 \\ 0 & 0 & L & 0 & 0 & M \\ M & 0 & 0 & L & 0 & 0 \\ 0 & M & 0 & 0 & L & 0 \\ 0 & 0 & M & 0 & 0 & L \end{pmatrix} \tag{8}$$

$$\begin{array}{ll} (1-D_{abc12})[i,i] & = 1 - Dk_i \\ (1-D_{abc12})[i,j] & = 0 \quad \text{if } i \neq j \end{array} \tag{9}$$

with $k_i \in \{a1, b1, c1, a2, b2, c2\}$

$$\begin{array}{ll} \text{sign}(I_{abc12})[i,1] & = 1 \; if \; Ik_i > 0 \quad else \; 0 \\ \text{sign}(I_{abc12})[i,2] & = -1 \; if \; Ik_i > 0 \quad else \; 0 \end{array} \tag{10}$$

The equations of C2IV are finally obtained in eq.11

$$\begin{aligned}
\frac{dI_{abc12}}{dt} &= [L \quad M]^{-1} \cdot \left(-R_L \cdot I_{abc12} + \begin{bmatrix} I_3 \\ I_3 \end{bmatrix} \cdot V_{xabc} \right. \\
&\quad \left. -(1-D_{abc12}) \cdot \text{sign}(I_{abc12}) \cdot V_{c12}\right) \\
\frac{dV_{c12}}{dt} &= \frac{1}{C} \cdot \left(\text{sign}(I_{abc12})^T \cdot (1-D_{abc12}) \cdot I_{abc12} - I_{out}\right) \\
\frac{dI_{abc}}{dt} &= \frac{1}{Lg} \cdot \left(V_{abc} - Rg \cdot I_{abc} - (V_{xabc} - \frac{1}{3} \cdot \sum V_{xabc})\right) \\
\frac{dV_{xabc}}{dt} &= \frac{1}{Cx} \cdot (I_{abc} - [I_3 \quad I_3] \cdot I_{abc12})
\end{aligned} \tag{11}$$

2.3 Rectifier Control

C2IV Rectifier control has a classic cascaded three loops topology, as shown in Fig.5:

1. An inner loop on input currents I_{abc12} is used to control the Power Factor (PF) and Total Harmonic Distortion of input currents (THD);
2. An outer loop on total output voltage V_{dc} is used to regulate V_{dc} for a wide range of output power;
3. A third loop on the output midpoint voltage V_{mid} is used to balance the two output voltages.

As one can often find in the literature, the outer loop controller is a PI with the peak input current as output. The third loop controller is a Proportional controller which adds an offset on duty-cycles. These loop are relatively slow.

The inner loop can be made in three different coordinate systems :

1. In dq-frame (I_d, I_q) as in (Liu et al., 2017b) (Tang et al., 2018), (Lai et al., 2009), (Ji et al., 2019) and (Liu et al., 2017a) to take advantage of a constant reference;
2. In αβ-frame (I_α, I_β) as in (Liu et al., 2018) to reduce control variables without using a complex PLL like in dq-frame;
3. In abc-frame (I_a, I_b, I_c) as in (Kolar and Friedli, 2011) and (Leibl, 2017) for simplicity.

Usually, a PI controller is used in dq-frame. A PI controller in abc-frame has been chosen for this application to simplify controller tunning. Moreover, abc-frame could be more robust to a phase loss because each phase is controlled independently.

Double carrier-based PWM is usually chosen (Liu et al., 2017b), (Tang et al., 2018), (Ji et al., 2019) and (Liu et al., 2017a). However a single carrier-based PWM has been chosen for simplicity. It compares duty-cycles from the output of inner loop with a single carrier. This choice is made possible by the use of the absolute value of currents as shown in Fig.5.

FPGA's capability allows a PWM sampling at 50 MHz. It suppresses the usual PWM sampling delay. Nevertheless the command, once changed by PWM algorithm, must be blocked until the end of half of the switching period to avoid command flickering.

The absolute currents reference in the inner loop is given by eq.12 :

$$\left|I_{abc_{ref}}\right| = I_{peak} \cdot |I_{sinus}| \tag{12}$$

The absolute sinusoidal shape is given by eq.13 :

$$|I_{sinus}| = \frac{|V_{xabc}|}{V_{xpeak}} \tag{13}$$

As the measurements of voltage V_{xabc} can be noisy, an observer has been preferred. The eq.14 shows the relation between input and output voltages and duty-cycle for Boost-converter over one phase.

$$|V_{xabc}| = (1-D_{abc12})[k,k] \cdot V_{c12} \tag{14}$$

The output voltages V_{c12} has been simplified by half of the reference value of the total output voltage $\frac{V_{dc_{ref}}}{2}$. The peak input voltage V_{xpeak} has been simplified by considering the maximum of the input voltages filtered measurements, which is about 95% of peak input voltage in three-phase. Thus the sinusoidal shape is built like shown in eq.15.

$$|I_{sinus}| = \frac{V_{dc_{ref}}}{2} \cdot \frac{1}{\max(V_{xabc})} \cdot (1-D_{abc12}) \tag{15}$$

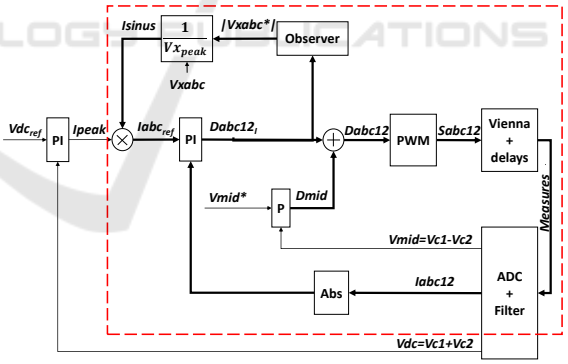

Figure 5: Control block diagram of C2IV Rectifier.

3 CURRENT LOOP STABILITY ANALYSIS

Linearising model of eq.11 around an operating point, the linearised state space of C2IV Rectifier is obtained in eq.16 :

$$\begin{aligned}
\dot{X} &= AX + BU \\
Y &= CX + DU
\end{aligned} \tag{16}$$

with the definitions of vectors in eq.17 :

$$\begin{array}{c} \text{State Vector} \quad X = (I_{abc12} \quad V_{c12} \quad I_{abc} \quad V_{xabc}) \\ \text{Command Vector} \quad U = (D_{abc12} \quad D_{mid}) \\ \text{Output Vector} \quad Y = (|I_{abc12}| \quad V_{mid}) \end{array} \tag{17}$$

Once this linearized state space obtained, one can draw the Bode Diagram between duty-cycles and input currents, study resonances and stability margins.

3.1 Input Filter Resonance Issue

Fig.6 shows that the current loop bandwidth does not depend on phase voltage. Indeed, the three curves corresponding to input voltages $(311V, -68V, -243V)$ are superimposed for frequency above 1kHz.

There are 3 resonances related to hardware input parameters L_g, C_x, and leakage inductance L_f (cf. eq.18) of coupled boost inductances. One zero z_1 (cf. eq.19) and two poles w_1 (cf. eq.20) and w_2 (cf. eq.21).

$$L_f = \frac{L-M}{2} \tag{18}$$

$$z_1 \simeq \frac{1}{2\pi \cdot \sqrt{C_x \cdot (L_g + L_f)}} \tag{19}$$

$$w_1 \simeq \frac{1}{2\pi \cdot \sqrt{C_x \cdot L_f}} \tag{20}$$

$$w_2 \simeq \frac{1}{2\pi \cdot \sqrt{C_x \cdot \frac{L_g \cdot L_f}{L_g + L}}} \tag{21}$$

Resonances at w_1 (20) and w_2 (21) are poorly damped. They are located above 10kHz, near the switching frequency. It implies that the control model cannot efficiently damp these resonances.

Furthermore, resonances move the location of stability margins to higher frequency, nearer to instability.

A passive damping must be added to avoid potential oscillations and increase stability margins.

Switching frequency (cf. f_{sw} in Table 1) limits already the current loop bandwidth at 11kHz. The presence of z_1 limits further the bandwidth at 2kHz for high grid inductance.

Control parameters of Table 2 have been chosen for this application.

The bode diagram of open current loop has been drawn in Fig.7 combining transfer function of Fig.6 and transfer function of PI controller (cf. eq.22).

$$H_{PI}(s) = K_p \left(1 + \frac{1}{T_i s}\right) \tag{22}$$

A gain margin of 14dB and a phase margin of 36deg are acceptable margins.

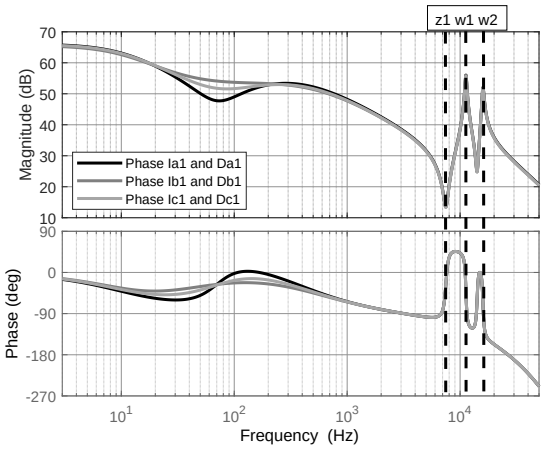

Figure 6: Bode diagram between the three first duty-cycles D_{a1}, D_{b1}, D_{c1} and their corresponding input currents I_{a1}, I_{b1},I_{c1}.

Table 2: Control Parameters.

Control Parameters	Value
Current Loop PI Gains	
Proportional Gain K_{pI}	5×10^{-3}
Constant Time Integral Gain T_{iI} (s)	4×10^{-5}
Total Voltage Loop PI Gains	
Proportional Gain K_{pV}	2.5
Constant Time Integral Gain T_{iV} (s)	1.3×10^{-3}
Midpoint Voltage Loop P Gain	
Proportional Gain K_{pM}	2×10^{-3}

Fig.7 also shows that phase margin is calculated after high frequency resonances instead of around 2kHz where gain crosses first time at 0dB. The resonances are clearly not enough damped. As w_1 and w_2 depend mainly on capacitors C_x and leakage in-

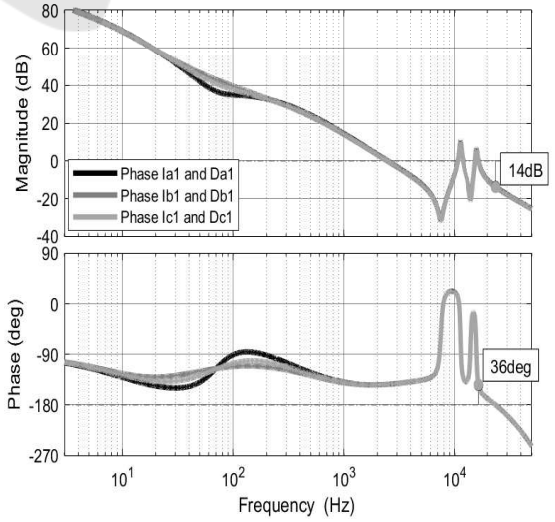

Figure 7: Bode diagram of open loop current control.

ductance Lf, a parallel damping circuit can be added to one of these components.

A RC circuit in parallel with capacitors could be the best good option. Indeed, the resistance R damps the resonance. The capacitor C helps to decrease the damping circuit losses by filtering low frequency harmonics coming from the grid.

Fig.8 shows the effect of a resistor R_x of 250mΩ in series with each capacitor C_x (cf. Fig.3). Resonances are clearly damped. Phase margin is calculated here around 2kHz.

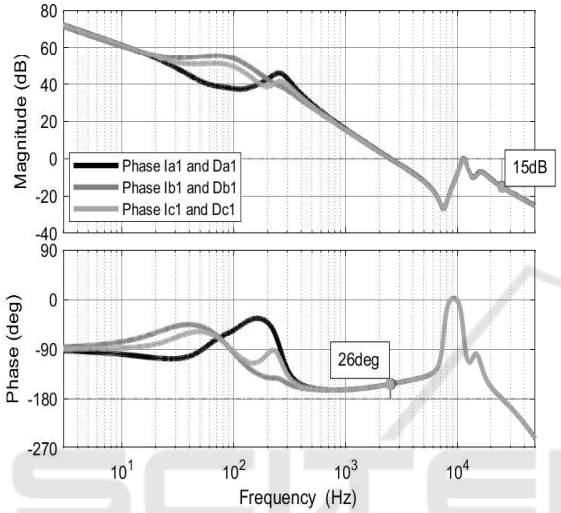

Figure 8: Bode diagram of open loop current control with input filter damping.

Nevertheless, damping three-phase input filter requires a study in itself and there is an extensive literature on this subject.

For the rest, only a damping resistor of 3mΩ has been added to take into account the parasitic resistors of the real capacitors implemented on the prototype.

3.2 Stability Analysis

The variable parameters of Table 1 modify stability margins. To understand where are the less stable operating points, these margins have to be calculated for all the domain.

The process of Fig.9 have been used to get the stability margins for all the operating points. A simulation model has been used to find a stable operating point for each choice of L_g, P_{out} and V_{in}. Then, the model has been linearised around these operating points. Transfer function between duty-cycle and input current have been obtained. Finally the margins of open loop transfer function are calculated and compiled.

Fig.10, 11 and 12 show that the worst operating

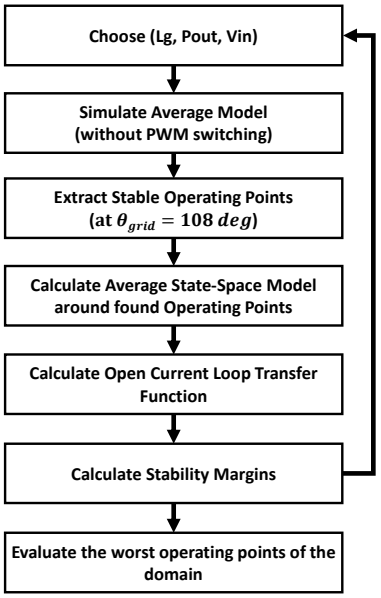

Figure 9: Process to obtain Stability Margins from the model and control of C2IV.

point considering stability margin is with low grid inductance, high nominal input voltage and low output power. The margins for the point $(L_g, V_{in}, P_{out}) = (10\mu H, 520Vrms, 10kW)$ are :

$(Gain, Phase, Delay) = (8dB, 25deg, 3.5\mu s)$

The minimum values of gain and phase margins are acceptable.

However delay margins are particularly low. Indeed, a synchronized PWM would have a zero order hold (zoh) at twice the switching frequency ($T_{zoh} = 22\mu s$) for interleaved rectifier. This would add a delay at twice the period of the zoh ($delay_{zoh} = 11\mu s$), which is greater than the minimum delay on the domain.

Fig.10 shows that stability margins hardly depend on grid inductance L_g. Indeed, leakage inductance L_f is very small compared to L_g almost everywhere in the domain. In this case, resonances w_1 (cf. eq.20) and w_2 (cf. eq.21) are approximately equal and independent from L_g.

Fig.11 shows that margins doesn't depend much on V_{in}, particularly for a low inductance L_g. For example, the gain margin range for a sweep of V_{in} varies from less than 1dB to 5dB.

Fig.12shows that margins depends more on P_{out}. For example, the gain margin range for a sweep of P_{out} varies from 7dB to 10dB.

The curves of phase and delay margins of Fig.12 show a discontinuity between 40kW and 50kW for $(L_g, V_{in}) = (10\mu H, 340V)$. It is explained by the fact that margins are calculated for a frequency above w_2

(cf. Fig.7) at low power. However depending on operating points, the minimum margin can be calculated for a frequency below w_2.

Hence C2IV control should stay stable at every operating point. However a better delay margin would be preferable. This can be achieved by the damping of input filter resonances.

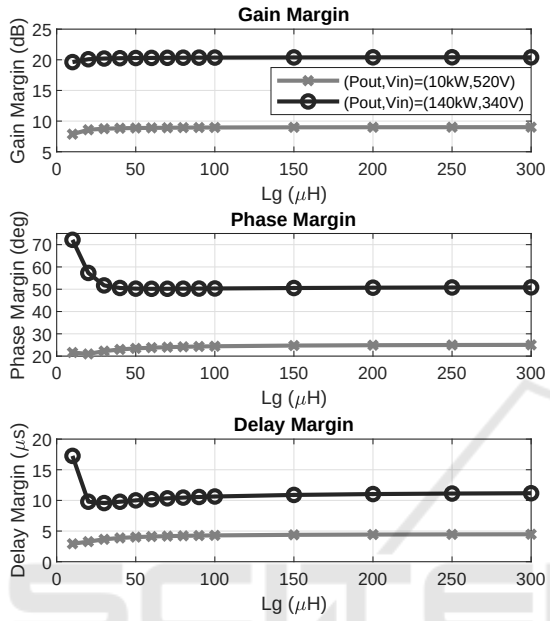

Figure 10: Upper and lower bound of current loop stability margins for a sweep of L_g.

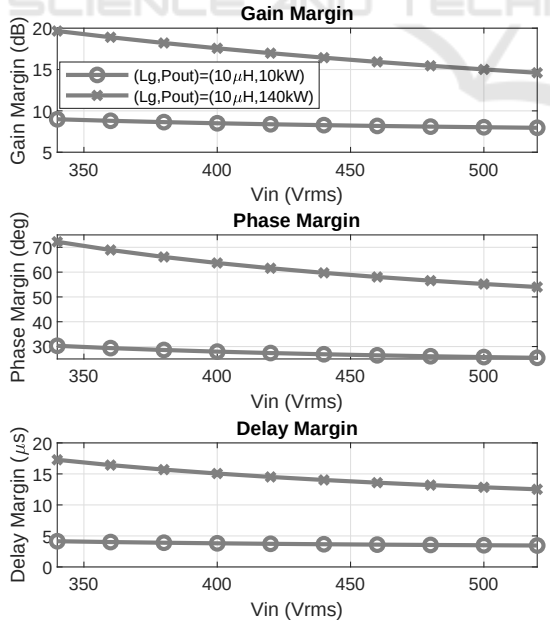

Figure 11: Upper and lower bound of current loop stability margins for a sweep of V_{in}.

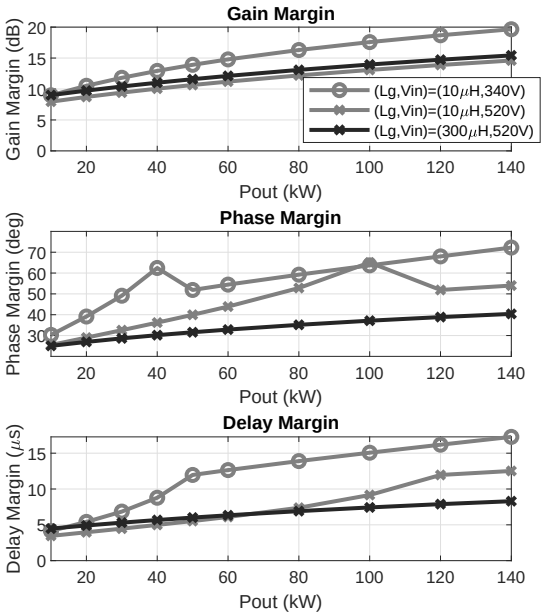

Figure 12: Upper and lower bound of current loop stability margins for a sweep of P_{out}.

4 MODEL VALIDATION

A comparison between measurements over a prototype and a Simulink-based Simulation has been made to validate model of eq.11.

The parameters are taken from Table 1. Values of the variable parameters for the comparison case are shown in Fig.13. A resistive load has been connected at the output of C2IV to make a power step from 1kW to 60kW. It allows a comparison of the system dynamic of the control of output voltage V_{dc} in Fig.14 and input currents I_{a1} in Fig.15.

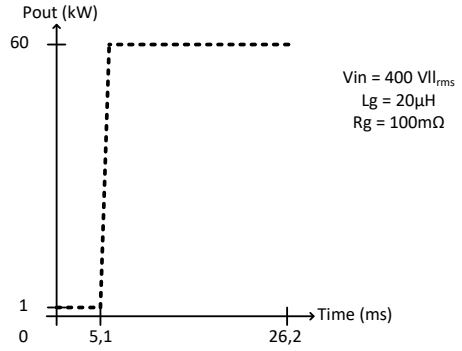

Figure 13: Load step specification.

The absolute error between measurements and simulation data have been drawn to have a closer look at the differences between them. To remove harmonics due to the switching frequency, a filtering have

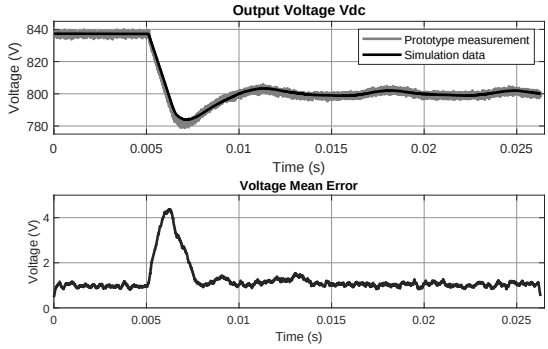

Figure 14: (Up) Output voltage V_{dc} from prototype measurement and simulation data. (Down) Filtered absolute error between prototype and simulation voltage.

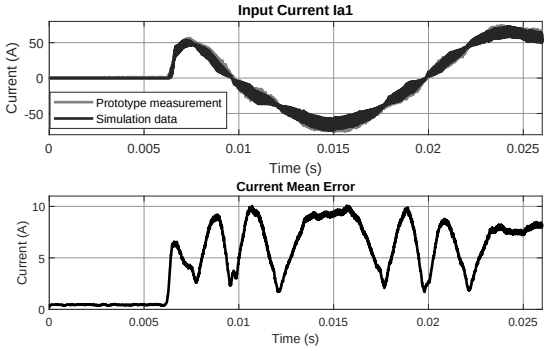

Figure 15: (Up) Input current I_{a1} from prototype measurement and simulation data. (Down) Filtered absolute error between prototype and simulation current.

been performed on the absolute error according to eq.23. A moving average over a window of 0.2ms has been used :

$$\varepsilon_{avg}[j] = \frac{1}{2N+1} \sum_{k=-N}^{+N} |X_{meas}[j+k] - X_{sim}[j+k]| \tag{23}$$

with N chosen as in eq.24 :

$$N \cdot T_{sampling} = 1 \times 10^{-4}\text{s} \tag{24}$$

Fig.14 shows that prototype measurements is very noisy. The error is up to 4.4V corresponding to the minimum of Vdc. This difference corresponds to some neglected losses which are not significant.

Fig.14 highlights that output voltage is not regulated well at no load. However voltage stayed within the $+/-50$V safety boundaries. This is acceptable for no load condition.

Fig.15 shows the effects of coupling inductances for both simulation and measures. Current ripple amplitude is varying from nearly 0A to 30A depending on the duty-cycle. As a consequence, currents in boost inductances will enter Discontinuous Conduction Mode (DCM) at low power. In fact, stability margins have been calculated with the hypothesis of Continuous Conduction Mode (CCM) for all power. Thus a stability analysis at DCM operation must be performed for low power.

The mean error is oscillating between 2A and 10A. This error can be explained by the poor synchronization of the high-frequency current oscillations between prototype measurement and simulation data. That does not matter for this study.

Fig.15 doesn't show a resonance around 10kHz, as could be expected by analysis of section3.1. This can be explained by the fact that damping parasitic parameters have been neglected. Thus resonance are well damped in reality. Nevertheless, these resonances have great chance to be excited. A known damping has to be added to prevent this case to happen.

The differences are sufficiently low, which allows to validate the model of C2IV.

5 CONCLUSIONS

Current loop stability study has highlighted that input filter parameters of C2IV introduce potential resonances in the system and modify stability margins. Although gain and phase margins are acceptable for all operating points, delay margin is very low at low power and at high input voltage. Adding a passive damping is the preferred option to prevent oscillations and move the margins to a more stable location.

Thus stability of the current loop of Vienna-type rectifier has been proved on a wide range of operating points. Weaknesses related to input filter have also been identified.

Future work can improve stability study by using a multi-variable approach, like H∞ methods with small gain theorem and μ-analysis.

Stability of Discontinuous Conduction Mode is another field of study. Coupled Inductances makes this study a challenge for modelling current loop adequately.

C2IV Rectifier show promising robustness performance on all operating points. It can meet the increase demand of pulsed power for Imaging Systems.

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