Integrated 16-Channel Neural Recording Circuit with SPI Interface and Error Correction Code in 130Nm CMOS Technology

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Abstract: In the research of neural diseases like epilepsy and schizophrenia genetic mouse models play a very important role. Dysfunctions during early brain development might cause these diseases. The analysis of the brain signals is the key to understand this process and develop treatments. To enable the acquisition of brain signals from neonatal mice, an integrated circuit for neural recording is presented. It is minimized for low area consumption and can be placed in a miniaturized system on the head of the mouse. It is intended to acquire the local field and action potentials from the brain. 16 analog input channels are implemented. The biomedical signals are amplified with analog pre-amplifiers. Two parallel structures of 8:1 multiplexer, post-amplifier and ADC are implemented to digitize the signals. The post-amplifier has programmable gain and high driving capability. The ADC is implemented as a 10 bit SAR ADC. Digital SPI interfacing is used to reduce the number of transmission lines. Reed Solomon Error Correction Coding has been implemented to enable error correction. The mixed-signal integrated circuit has been successfully implemented in a 130 nm CMOS technology. It is optimized for low area consumption; the channel density is approximately 10 channels/mm^2.

1 INTRODUCTION

In the development of treatments for diseases like epilepsy, schizophrenia or autism spectrum disorders (ASD), the neural recording of the signals from the brain from neonatal mice plays a key role. The development of the brain and its neural networks is a complex process in which neurons are born, migrate and establish synaptic connections (Ben-Ari et al., 1997). The neurodevelopmental hypothesis suggests that neurological diseases can arise from dysfunctions during early brain development (Lewis and Levitt, 2002). Genetic mouse disease models are used to investigate this hypothesis and to development treatments against this diseases. The brain signals of the mice are recorded and analysed at neural level. Of special interest are neonatal mice, since the diseases develop in this period. Neonatal mice are very small and have a body weight of only 3-5 g.

For the neural recording, microelectrodes are inserted into the cortex of mice. The microelectrodes are connected to the integrated circuit. The integrated circuit amplifies and digitizes the signals. The system of microelectrodes and integrated circuit will be placed on the head of the mouse. This system is connected to the recording system with wires. Due to the small size of the neonatal mice, the size of the integrated circuit has to be minimized. To reduce the constraints in the behaviour, the wiring has to be reduced as much as possible.

Every analog transmission is a potential source of noise and distortion to a signal. As soon as the signal is digitized, theoretically it can be transferred without any errors. Because of this it is of high importance to digitize the signals as close to the brain of the mouse as possible. In this context the presented integrated circuit provides the best possible solution. It can be placed on a miniaturized system directly next to the electrode.

The presented integrated circuit is optimized for the signal acquisition of extracellular action potentials (AP) and local field potentials (LFP). The LFP are typically measured in the range up to 300 Hz, AP in the range up to 10 kHz. The amplitude range is up to several millivolts for LFP and hundreds of micro volts for AP.

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2 SPECIFICATION AND SYSTEM DESIGN

There are several approaches for the acquisition of neural activity described in different ways in literature: monopolar, bipolar or tri-polar recording. A widely used bipolar circuitry is described in (Harrison and Charles, 2003). Advantages of bipolar signal acquisitions are better symmetry for the input circuit and higher common mode rejection ratio (CMRR). Disadvantages are the higher number of electrodes and cables, resulting in double the number of input and output (IO) pins and electrostatic discharge (ESD) pads on the integrated circuit. Since area reduction is one of the main goals of this circuit, a monopolar recording is chosen to be implemented.

The integrated circuit is connected to commercially available silicon-based microelectrodes ('silicon probes' e.g. from NeuroNexus and Acreo). The measured noise level from the microelectrodes is typically V_{noise} = 15 μV_{rms} (NeuroNexus, 2013). The noise of the microelectrodes and the noise of the integrated circuit compose the system noise of the signal acquisition system. The integrated circuit is designed in such a way that the system noise is greatly determined by the noise of the microelectrodes. The ADC quantization noise is much smaller than the noise level of the microelectrodes.

The technology chosen is a 130 nm CMOS technology, which reduces the area compared to commercial available systems. The widely used integrated circuits from the company Intan Technologies require an area of approximately 20 mm². From the desired application, these design specifications for the system are derived:

- Technology: 130 nm;
- Analog Inputs: 16;
- Noise (input referred): 3.4 μV_{rms} (2 – 10 kHz);
- Input Range: ±8, ±6, ±3, ±1.5 [mV];
- Bandwidth: 2 Hz – 10 kHz;
- ADC Resolution: 10 bit;
- Sampling Rate: 20 kS/s/channel;
- Effective area < 1.8 mm²

A system block diagram of the integrated circuit is shown in Fig. 1. The system comprises 16 channels. In the first stage the signals are amplified by low-noise preamplifiers with a gain of approximately 34 dB.

A multiplexer connects 8 pre-amplifiers to a post-amplifier. The post-amplifier is connected to a successive approximation register ADC. This post-amplifier has a programmable gain and has to be very fast to charge the capacitors of the ADC (Bahr et al., 2015).

For the digital interfacing to the integrated circuit a bidirectional serial peripheral interface (SPI) is implemented. Error Correction Coding (ECC) is implemented to enable correction of bit errors caused by reflections on the transmission lines.

Each channel of the system is able to record signals up to $f_{bandwidth}$ = 10 kHz. According to the Nyquist criterion, the minimal channel sampling frequency is $f_{sample} = 2 * f_{bandwidth}$ = 20 kHz. With N = 16 channels the minimal required sample rate is sample rate = N * f_{sample} = 320 kSamples/s.

The SAR ADC requires k = 14 cycles to produce 10 bits per sample. Hence the minimal ADC frequency $f_{ADC, min}$ can be calculated as:

$$f_{ADC, min} = k * \text{sample rate} = 4.48 \text{ MHz}. \quad (1)$$

The use of a single multiplexed structure connected with 16 pre-amplifiers would require the ADC to have a frequency of $f_{ADC, min}$ = 4.48 MHz. Furthermore the post-amplifier has to charge the ADC in t ~ 1/ $f_{ADC, min}$.

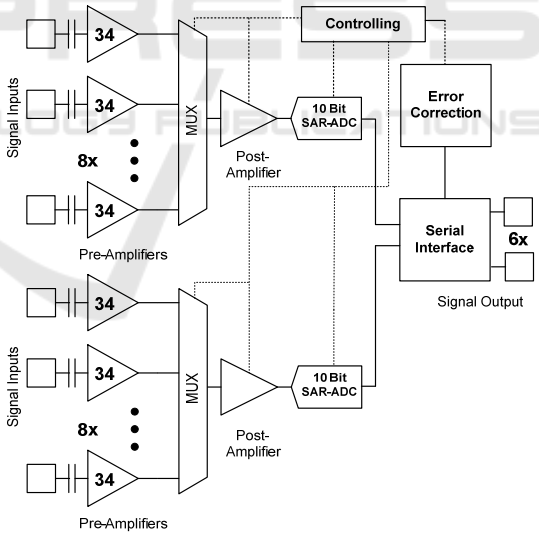

Figure 1: Block diagram of the integrated circuit with 16 analog inputs and digital output.

To ease the specifications, a parallel structure of one post-amplifier and one SAR ADC each connected to 8 pre-amplifiers is chosen. This reduces the minimal required operation frequency of the ADC by 50% to $f_{ADC, min}$ = 2.24 MHz and doubles the time for the post-amplifier to charge the ADC´s input capacitance.

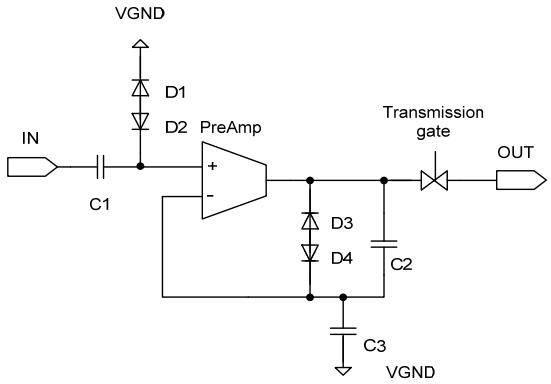

Figure 2: Schematic of the pre-amplifier.

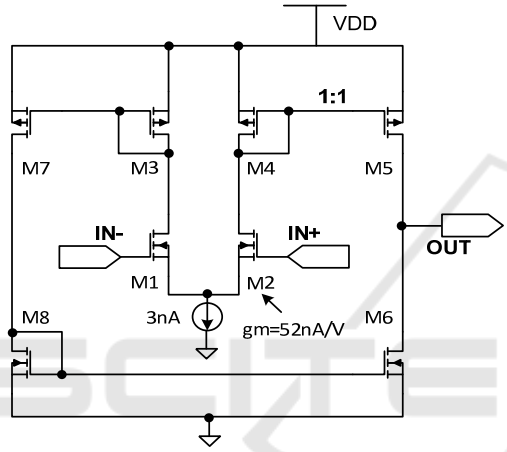

Figure 3: Circuit of the symmetrical operational transconductance amplifier used in the pre-amplifier.

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2.1 Pre-amplification

The circuit of the pre-amplifier is shown in Fig. 2. To avoid the large DC voltage, which occurs at the input in biomedical signal acquisition and might drive the amplifiers into saturation, capacitive coupling is used. The size of the input capacitance is C1 = 3 pF.

The size of the capacitor in the feedback loop is only C2 = 85 fF. The feedback loop is connected via C3 = 5.2 pF to the common reference VGND.

Resistors in the high GΩ range require large areas. To overcome this, two diodes connected in reverse direction are chosen to reduce the area consumption of the preamplifier. They consume only an area of A = 2 * w_{diode} * l_{diode} = 2 * 4 µm * 0.65 µm = 5.2 µm^2.

The circuit of the realized operational transconductance amplifier is depicted in Fig. 3. The transistors M1 and M2 operate in the sub-threshold region for minimal power consumption and optimal noise characteristic.

With this design an overall power consumption of P_{tot} = 29 µW is achieved for the pre-amplifier.

The gain of the pre-amplifier is set to 34 dB with a bandwidth of 2 Hz to 10 kHz. The input referred integrated noise voltage of the pre-amplifier is 3.4 μV_{rms} in the range of 2 Hz to 10 kHz.

2.2 Multiplexer

Two 8:1 multiplexers are implemented in the integrated circuit. Each multiplexer is switching 8 channels in a synchronous and continuous way to the post-amplifier. The switches are implemented by using transmission gates. They are controlled digitally and synchronized to the clock of the ADC.

2.3 Post-amplification

The post-amplifier matches the pre-amplified and multiplexed signal to the input range of the ADC of VDD = 1.2 V. It charges the capacitor array of the SAR ADC in the given time period. Derived from the specification, a rail-to-rail amplifier with programmable gain is chosen (Tomasik, 2008).

Fig. 4 shows the circuit of the pre-amplifier. The programmable gain is implemented by switchable resistors R1 to R4 in the feedback loop.

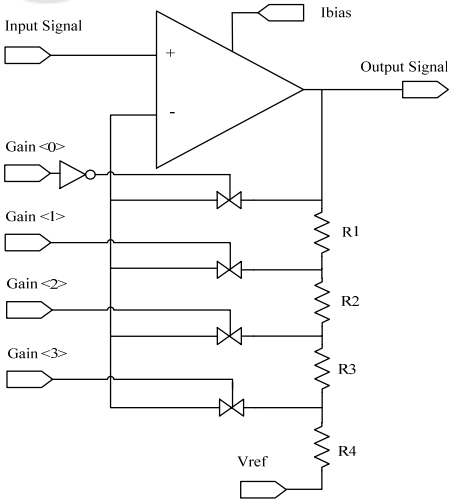

Figure 4: Schematic of the post-amplifier.

The gain of 0, 6, 12 and 18 dB is realized by voltage dividers of poly resistors. The settings of the switches are controlled by a configuration registers. The default setting is set to an amplification factor of one.

2.4 A/D Conversion

For analog to digital conversion a 10 bit successive approximation register (SAR) A/D converter is implemented.

The capacitor array of the ADC is built of unit capacitances of C_{unit} = 63 fF. The total capacitance sums up to C_{total} = 64.5 pF. The total area of a SAR ADC is significantly determined by the size of the capacitor array. The area of the implemented ADC is A = 375 µm * 360 µm = 0.135 mm^2.

The SAR ADC requires 14 cycles to produce the 10 bits per sample. The ADC frequency is f_{ADC} = N/2 * f_{sample} * 14 cycles/sample = 2.24MHz.

Using a supply voltage of VDD = 1.2 V the resolution of the 10 bit ADC is ΔV = 1.17 mV. This corresponds to a system input referred resolution of ΔV = 0.84 μV_{rms}. The resolution is much smaller than the noise level of the electrodes of V_{noise} = 15 μV_{rms}.

2.5 Digital Block

The digital part of the integrated circuit implements a configuration register, a SPI slave module for data communication and configuration of the integrated circuit as well as a Reed Solomon Error Correction Code module.

2.5.1 Configuration Register

The modular design of the integrated circuit requires a memory block to save the settings for the signal acquisition. This element is implemented as a 20 bits long shift register, which is accessible by the bidirectional SPI interface. The register stores the following parameters:

- Enabling of the Error Correction Coding module,
- Enabling of Multiplexers,
- Amplification of the post-amplifiers (4bit). The same post-amplification factor is applied to all 16 channels.

The default settings for the controlled blocks are designed in such a way that the integrated circuit is in a defined and usable state after a reset, in which all its bits are set to zero. This increases design robustness against single points of failure and allows the test of the circuit even without a configuration written.

2.5.2 SPI Slave Module

The integrated circuit is designed to enable signal acquisition on moving subjects, which are connected to the recording unit with cables. Thus, reducing the number of wires is crucial. Furthermore, every connected wire requires extra area on the integrated circuit for bond pad and ESD structure.

Differential signalling of the IOs is more robust and power efficient than single ended signalling. But, it requires double the number of wires and area on the integrated circuit. To achieve maximal reduction of area and wiring, single ended signalling is chosen.

The integrated circuit implements a slave in a so called four wire SPI with the signals:

- SCLK – Serial Clock
- CS – Chip Select
- GR – Global Reset
- MOSI – Master Out Slave In
- MISO – Master In Slave Out

The connection of the digital I/O is shown in Fig 5. The End of Conversion (EoC) signal from the SAR ADC indicates the finalization of each A/D conversion and is used as an interrupt for the SPI master.

The signal global reset does not require a wired connection to the SPI master. In a miniaturized system it is hardwired to V_{DD}.

In total, the integrated circuit requires only 5 wires for digital communication compared to 16 wires for an analog signal acquisition.

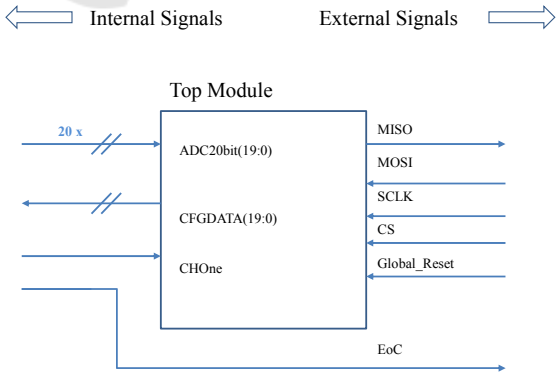

Figure 5: Signal diagram of the digital block of the integrated circuit.

The SPI master controls the SPI slave using a 22 bit word. The first two bits are used as command bits;

Table 1: Commands to control the SPI slave.

Bit pattern	mode of operation
'00'	IDLE state
'01'	write (write the MOSI data into the configuration register)
'10'	read the ADC data (20 bit or 36 bit, depending on system configuration)
'11'	read configuration register

Table 2: Data package structure sent by SPI slave.

Number of bits in this order	Meaning
1 bit	Indicating if channel 1 is sent
1 bit	Indicating if ECC is active
20 bit	Data from ADC (10 bit each)
16 bit	16 bit: Error Correction Codes (If ECC module is active)

the next 20 bits are optional for configuration data. The commands for the modes of operation are shown in Tab. 1.

To enable high density neural recording daisy chaining of several integrated circuits is enabled. The SPI Interface works at a maximum frequency of f_{SPI} = 25 MHz.

The required bit rate for one integrated circuit with a sample rate = 320 kSamples/s and a packet size p_{size} is:

$$\text{bit rate} = p_{size} * \text{sample rate}. \quad (2)$$

The maximal packet size is $p_{size,max}$ = 38 bit (2 control bits, 2 samples with 10 bits, 16 bits ECC). This gives a bit rate of bit rate_{max} = 6.08 Mbit/s. At this bit rate it is possible to daisy chain four integrated circuits. With four integrated circuits 64 analog channels can be acquired.

For a data packet size of $p_{size,noECC}$ = 22 bit (2 control bits, 2 samples with 10 bits) the bit rate per integrated circuit is bit $\text{rate}_{size,noECC}$ = 3.52 Mbit/s. This enables the daisy chaining of 7 integrated circuits.

With a system of seven integrated circuits 112 analog channels can be acquired. In this system the length of the 112 analog transmission lines is reduced to short bond wires between microelectrodes and integrated circuit. For the data transmission from the miniaturized system to the receiver only 11 digital wires are required. Thus a significant reduction in wiring of approximately 10:1 is achieved.

2.5.3 Error Correction Codes

The high data acquisition rate of the integrated circuit requires high data transmission rates to the host module. In high speed data transmission, reflections can occur because of mismatch at the terminations of the transmission lines. The reflections can provoke bit errors. To correct these, an error correction mechanism is realized.

A Forward Error Correction adds additional redundancy to the data. This allows error correction at receiver side up to a certain degree of errors.

The integrated circuit implements Reed-Solomon Error Correction Coding (Tej and Rani, 2013) using the following parameters: m=4, n=9, k=5 and t=2.

Based on the primitive polynomial:

$$p(x) = x^4 + x + 1 \quad (3)$$

The used generator polynomial is:

$$g(x) = x^4 + 13\,x^3 + 12\,x^2 + 8\,x + 7 \quad (4)$$

With this implementation it is possible to correct up to 8 bit errors at receiver side in on data packet. The data packet structure is given in Tab. 2.

3 RESULTS

The integrated circuit was fabricated in a 130 nm CMOS process. A picture of the die of the integrated circuit is shown in Fig. 6.

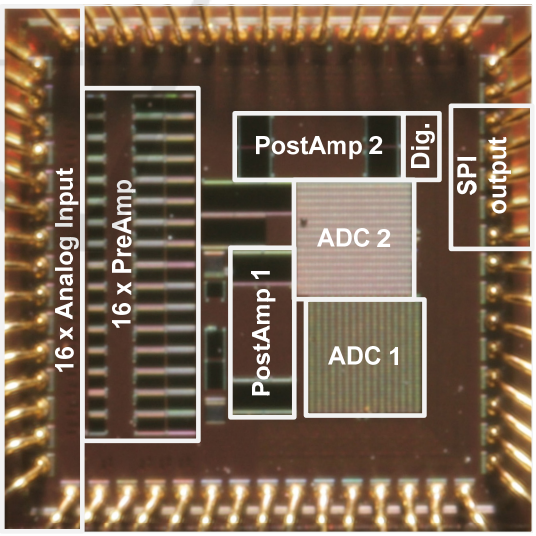

Figure 6: Picture of the die of the integrated circuit. Depicted are the analog I/O on the left and the digital I/O on the right side as well as the submodules.

The integrated circuit consumes an area of 1.525 * 1.525 mm^2. The spatial arrangement is divided into an analog and a digital block. On the left half of the die the analog blocks are placed: analog inputs, pre-

amplifiers and post-amplifiers. The digital blocks are ADCs (mixed-signal), digital module and SPI interface. For debugging purpose 22 test pins and further test structures are implemented.

The required area of the integrated circuit is A = 1.71 mm^2, including all necessary pads and ESD structures. This corresponds to a density of approximately 10 channels / mm^2.

The measured frequency response of the pre-amplifier is shown in Fig. 7. The gain is 34dB and the bandwidth 2 Hz to 10 kHz.

The output spectrum of a sinusoidal signal with amplitude V = 15 μV_{rms} and frequency f = 3 kHz is shown in Fig. 8. The signal was pre-amplified by 36 dB, post-amplified by 18 dB, digitized by the 10 bitSAR ADC and acquired via the SPI Interface.

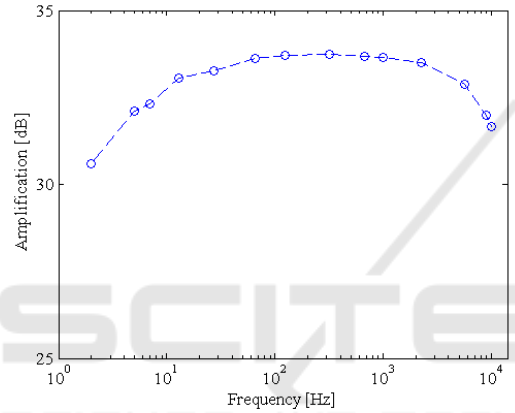

Figure 7: Frequency response of the pre-amplifier.

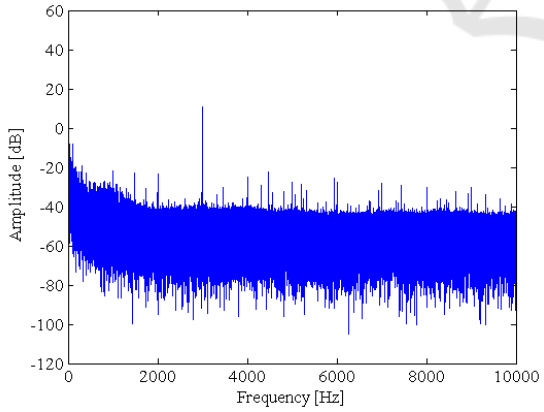

Figure 8: Spectrum of a sinusoidal input signal with amplitude V = 15 μV_{rms} and frequency f = 3 kHz.

4 CONCLUSIONS

An area optimized integrated circuit for neural signal recording has been successfully implemented in a 130nm CMOS technology. The circuit acquires the signals with 16 analog low-noise pre-amplifiers and provides the digitised data via a SPI interface.

The high channel density of 10 channels/mm^2 and the small size of the integrated circuit enable recordings of LFP and AP in close proximity to the brain. Daisy chaining of several integrated circuits allows high density recordings of up to 112 channels. This leads to a reduction of wiring for digital data transmission of 10:1 compared to analog data transmission.

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