On the Investigation of Lumped Parameter Models for Thermal Characterization of High Power Modules

Marco Iachello
Dipartimento di Ingegneria Elettrica Elettronica e Informatica, Facoltà di Ingegneria, Università degli studi di Catania, viale A. Doria 6, 95125 Catania, Italy

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Abstract: This research focuses on the development of a new thermal modelling methodology of multichip electronic power modules. The current stage of the research is intermediate. In the first step the implementation of simulations for collecting thermal data on high power modules has been performed. The current step is the development of the methodology for lumped parameter models extraction. The main aim of this project is to generate an optimized procedure for the design of lumped parameter thermal models extracted from 3D-field simulations or experimental measurements

1 STAGE OF THE RESEARCH

This research focuses on the development of a new thermal modelling methodology of multichip electronic power modules. The current stage of the research is intermediate. In the first step the implementation of simulations for collecting thermal data on high power modules has been performed. The current step is the development of the methodology for lumped parameter models extraction.

2 OUTLINE OF OBJECTIVES

The main aim of this project is to generate an optimized procedure for the design of lumped parameter thermal models extracted from 3D-field simulations or experimental measurements.

3 RESEARCH PROBLEM

The growing demand of high power devices concentrated in small volumes is leading to the design of integrated power modules. They are realized by integrating several chips inside one package. Consequently the resulting high power density produces strong thermal constraints on the package. Furthermore, the different chips included in the device are thermally coupled, then the thermal power provided by each chip has the effects of heating the chip itself and all the other chips in the package. Thermal aspects become dominant and strongly influencing either the module working conditions or its lifetime. As a result the probability of failures, due to the thermal stresses, significantly increases, thus impacting on the reliability. Then to keep the device in safe operating conditions, the silicon chips junction temperature (both in transient and in steady-state regime) should be known and controlled. On the one hand, thermal simulators need to be more and more able to reproduce instantaneously the device thermal behaviour. On the other hand, if there are more than just a few chips thermally modelled the simulation time of three dimensional models increases enormously. The result is that a trade-off is necessary. This research addresses the problem to reproduce the thermal behaviour of high power modules by means of equivalent circuit simulators.

4 STATE OF THE ART

Many papers describing numerical methods for thermal analyses of multichip power modules have been published (Wu et al., 2013); (Shammas et al.,

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2002). In general it is possible to classify them in two main categories: approaches based on distributed parameter models and on lumped parameter models.

4.1 Distributed Parameter Models

Distributed parameter models are characterized by the fact that all variables are both function of time and function of some spatial coordinates.

Assuming constant thermal conductivity, the heat conduction inside a volume domain is described by the following equation (Cengel, 2002):

$$\nabla^2 T + \frac{\dot{g}}{\lambda} = \frac{1}{k}\frac{\partial T}{\partial t} \quad (1)$$

where t is the time, T the temperature field, k the thermal diffusivity, λ is the thermal conductivity and $\dot{g}$ the rate of the internal heat generation per unit volume. The equation (1) can be solved employing different methods as the Finite Element Method (FEM) and the Boundary Element Method (BEM). These approaches, which can be described as physical modelling, entail decomposing the device geometry into a collection of volume (FEM) or surface (BEM) elements (meshing), and then solving a system of partial differential equations for the field values at the element control points.

The problem is completed assigning initial and boundary conditions.

Typically power modules are made by thin vertical layers and have large horizontal dimensions. It means that the heat flux predominantly flows from the top to the bottom of the module. Consequently the flux through the lateral sides could be neglected and the corresponding boundary condition assigned is adiabaticity.

If the heat sink is dimensioned properly, it will be able to dissipate the whole heat and its bottom side could be assumed isothermal.

Let us consider a power module made up of n chips and focus our attention on its FEM thermal modelling.

As explained in (Khatir et al., 2004), the heat transfer problem could be assumed linear and this hypothesis is in good approximation true for most power electronic applications. Under these conditions the superposition principle is applied.

The usual approach (Drofenik et al., 2007); (Carubelli and Khatir, 2003) consists in applying a power pulse (P_i) only on a single chip and to measure thermal responses on all chips. The temperature of the bottom side of the heat sink is called reference temperature (T_r). The approach is schematically shown in Figure 1.

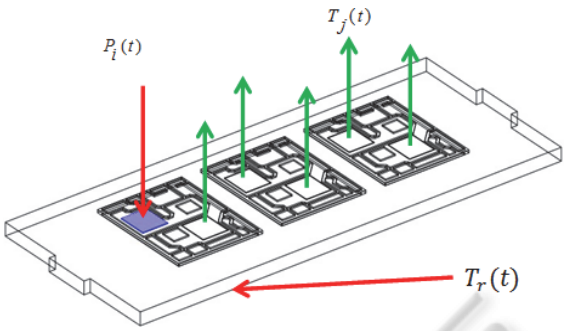

Figure 1: A prototypal version of a power module made of 6 IGBTs and 6 diodes.

To characterize the response of the heated chip, the so-called thermal self-impedance is defined:

$$Z_{th,ii} = \frac{T_i - T_r}{P_i} \quad (2)$$

where P_i is the power applied on chip i and T_i is the temperature of the centre, on the top area, of the heated chip i.

The thermal coupling effect between chips is given from the thermal mutual-impedance defined as:

$$Z_{th,ij} = \frac{T_i - T_r}{P_j} \quad (3)$$

where T_i $(i \neq j)$ is the temperature of the centre of chip i when chip j is heated by the power P_j.

Then, for a device having n chips, it is possible to assemble the following thermal impedances matrix:

$$Z_{th} = \begin{pmatrix} Z_{th,1,1} & \cdots & Z_{th,1,n} \\ \vdots & \ddots & \vdots \\ Z_{th,n,1} & \cdots & Z_{th,n,n} \end{pmatrix} \quad (4)$$

in which the coefficients of the main diagonal are the self-impedances of each silicon chip while the other terms are the mutual-impedances describing coupling effects between chips.

It is important to underline that thermal impedances can be calculated from 3D thermal model or extracted from experimental measurements.

Combining equations (2)-(4), the complete model can be written in matrix-form as:

$$Z_{th} P = \Delta T \quad (5)$$

where Z_{th} is the $n \times n$ thermal impedances matrix, P is the $n \times 1$ vector of the input powers P_i and ΔT is a $n \times 1$ vector of the differences between the temperature chip T_i and the reference temperature

T_r.

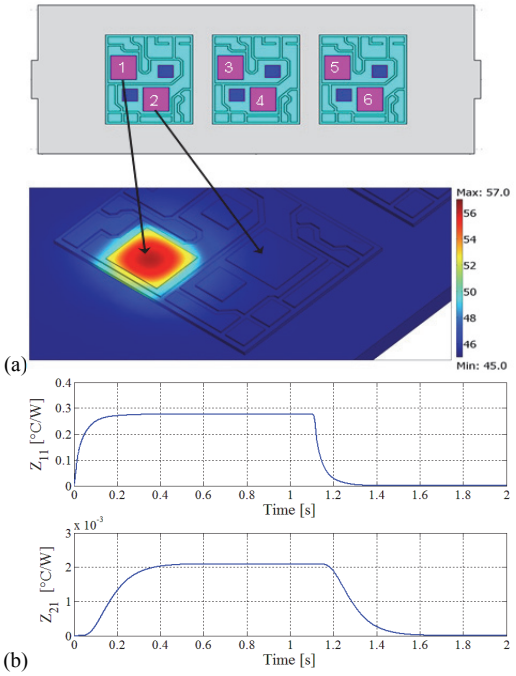

Figure 2: (a) Colormap of a 3D COMSOL Femlab thermal simulation. (b) Thermal self-impedance $Z_{11}(t)$ and mutual thermal impedance $Z_{21}(t)$ extracted from the simulation.

Figure 2 shows an example of the result of the methodology described above applied to a power module prototype. In this case the chip 1 is heated (Figure 2a) and the response of the chip 1 itself and of the chip 2 have been extracted.

Comparing the thermal impedances in Figure 2b the presence of a delay in the mutual impedance is evident.

Although 3D numerical simulations are very accurate, they can require very high computational cost and long simulation times.

4.2 Lumped Parameter Models

Starting from the thermal impedance curve, a thermal equivalent circuit can be designed. This is possible because there is an analogy between thermal and electrical quantities (Table 1).

Table 1: Analogy between thermal and electrical quantities.

Thermal Power	Electrical current
Temperature difference	Voltage difference
Thermal capacity	Electrical capacity
Thermal resistence	Electrical resistence

The main approaches to reproduce the thermal behaviour of semiconductor components are two (Infineon Ltd, 2008); (ABB Ltd, 2013): RC Cauer model and RC Foster model. Both of them use passive circuital network topologies.

The first one is the "RC Cauer" method and the correspondent circuit is shown in Figure 3. This approach is a realistic physical representation of single device thermal behaviour. Each RC cell describes the thermal behaviour of one module layer. The model can be set up only with the knowledge of the material proprieties of each individual layer characterizing the device.

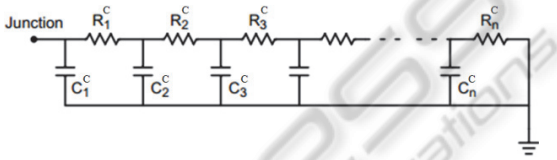

Figure 3: RC Cauer model.

The circuit nodes allow to access the internal temperatures of the layer series.

In contrast, the "RC Foster" approach, whose circuit is shown in Figure 4, is the most used because it is characterized by a simpler modelling procedure.

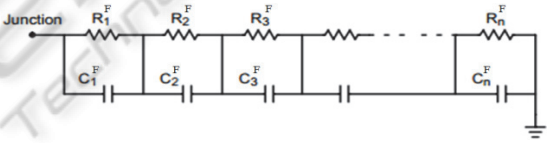

Figure 4: RC Foster model.

This approach simply consists of fitting the thermal impedance curve using the following relation:

$$Z_{th(j-c)}(t) = \sum_{i=1}^{n} R_i^F (1 - e^{-\frac{t}{\tau_i}}) \qquad (6)$$

where n is the number of RC cells and τ_i is the time constant of the i cell.

Comparing these two methods it is important to underline that the transformation from one to the other is always possible. This procedure is based on the transfer function representation.

For instance, the transformation of a Foster model made up by two RC cells into the Cauer one is given by the following equation:

$$Z_{th\_C} = \frac{1}{sC_1^F + \frac{1}{R_1^F + \frac{1}{sC_2^F + \frac{1}{R_2^F}}}} \qquad (7)$$

where Z_{th_C} is the thermal impedance in Cauer form and R_1^F, C_1^F, R_2^F, C_2^F are the Foster model coefficients.

Once obtained one equivalent circuit for every thermal impedance, equation (5) can be modelled in the circuit simulator following the procedure in (Drofenik et al., 2007). Specifically, if the dimension of the thermal impedance matrix is $n \times n$, the circuits are connected together forming a $n \times n$ circuits network.

5 METHODOLOGY

The main idea is to develop an automatic procedure to reproduce the thermal behaviour of power modules by means of lumped parameter models.

The methodology is based on different steps and starts from information collected on a distributed parameter model.

The first step is to obtain the thermal impedance curves characterizing the module thermal behaviour.

A way to get these information is the design of accurate thermal models of power modules by means of FEM tools.

This is also useful to understand the heat propagation dynamics through layers characterized by different materials. Understanding thermal dynamics is the preliminary step to model them opportunely.

Another way to get the thermal impedance curves is to perform experimental measurements on the device. This last aspect is also very significant to validate the thermal model.

Once the thermal impedances have been obtained, the next step is to find a passive circuit topology able to reproduce them.

Here, the problem has to be split in two subparts: the self-impedance fitting and the mutual-impedance one. While in the first case traditional approaches work well by using equation (6), for the mutual-impedances we have found that this is not always true, especially in the presence of large delays.

For instance, we have found that the analytical function:

$$Z_{th,ij}(t) = R_{ij}\left(1 - \frac{\tau_e}{\tau_e - \tau_s} e^{-\frac{t}{\tau_e}} + \frac{\tau_s}{\tau_e - \tau_s} e^{-\frac{t}{\tau_s}}\right) \quad (8)$$

used in (Khatir et al., 2004) and (Carubelli and Khatir, 2003) is not suitable for every type of mutual impedance.

By observing some 3D thermal simulations performed on a power module prototype it has been possible to draw some considerations.

In contrast to the self-impedance behaviour, in fact, the mutual impedances are affected by a delay which increases when the distance between chips grows.

This delay is visible in Figure 5 along with the RC network approximation of the thermal impedance curve. As it can be observed, the approximation is not satisfactory. At the current stage of our research, we are exploring new circuit topologies for better approximation. The preliminary results indicate that such models can be obtained in the realm of passive circuits.

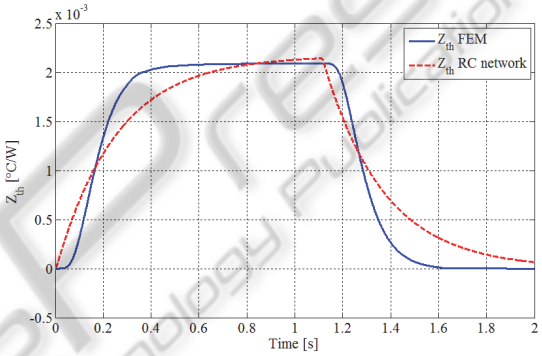

Figure 5: Thermal mutual impedance calculated from a 3D numerical simulation of a power module prototype (blue) and its fitting (red) by means of relation (8).

It is important to underline that the use of the FEM tool is only finalized to get the thermal impedances curves, so it will be used only once.

The aim of this research is to investigate alternative forms for fitting the thermal mutual impedances.

Then the thermal behaviour of the whole module will be characterized by the lumped parameter model.

6 EXPECTED OUTCOME

The aim of this work is to design an automatic procedure allowing a fast modelling of the whole module thermal behaviour.

Specifically the choice of the lumped parameter approach has many advantages. First of all, a circuit is more versatile than a 3D model that needs of specific tools to be simulated. Secondly, the computational cost required for a lumped parameter model is much lower than a distributed parameter one.

The thermal behaviour of power modules can change significantly depending on the density of chips, the used materials and the module geometry.

Starting from the thermal impedance curves, obtained by 3-D numerical simulation or by experimental measurements, the methodology will allow to find a suitable circuital network topology able to reproduce both the single chip behaviour and the thermal coupling between different chips.

In summary the main expected outcomes are two. The first one is the definition of a methodology to design lumped parameter models reproducing the thermal behaviour of high power modules.

The second expected outcome is the availability of particularly simply models for fast simulation of thermal behaviour of high power modules.

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