PULSE-TYPE NEURO DEVICES WITH TWO TIME WINDOWS IN STDP AND ITS APPLICATION TO THE MEMORY OF TEMPORAL SEQUENCES PATTERNS

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Abstract: Since neural networks have superior information processing functions, many investigators have attemptted to model biological neurons and neural networks. A number of recent studies of neural networks have been conducted with the purpose of applying engineering to the brain. Especially, neuro devices have been created that focus on how learning is achieved. Here, we focus on spike timing dependent synaptic plasticity (STDP) and construct pulse-type neuro devices with STDP. In this paper, we focus on two time windows in STDP, and we propose a synaptic weight generation circuit which indicates an asymmetric or a symmetric time window by changing voltages in the proposed circuit. As a result, we show that a pulse-type neuro device with two time windows in STDP stores temporal sequence output voltage patterns which conform to the temporal sequence input current patterns for memory.

1 INTRODUCTION

The classical Hebbian learning rule (Hebb 1949) is believed to play an important role in synaptic plasticity of neural networks in the brain. This rule uses mean spike firing correlations between pre- and postsynaptic neurons to drive learning. Recently, the form of synaptic plasticity dependent on the order and time interval of pre- and postsynaptic spikes (STDP: spike timing dependent synaptic plasticity (Bi and Poo, 1998) was observed in the hippocampus and cerebral cortex (Patrick and Curtis, 2002, Sakai and Yoshizawa, 2003). In general, STDP manifests itself as a potentiation of a synapse if the presynaptic spike precedes the postsynaptic spike, and as a depression if the presynaptic spike follows the postsynaptic spike (an asymmetric time window). In addition, it has been reported that the depression caused when the presynaptic spike precedes the postsynaptic spike (a symmetric time window) depends on the influence of an inhibitory neuron (Tsukada, Aihara, Kobayashi and Shimazaki, 2005). Furthermore, it has been reported that recall of two states (autoassociative and heteroassociative) using the two time windows in the mathematical model (Samura, Hattori and Ishizaki, 2008) exist.

On the other hand, hardware neuron models with STDP have been proposed based on the results of physiological experiments (Tanaka, Morie and Aihara, 2009 - Schemmel, Grubl, Meier and Mueller, 2006). Especially, the latest research has the purpose of being applied to engineering. For example, using analog circuits, associative memory(Tanaka, Morie and Aihara, 2009), vision model(Zhijun, Murray, Worgotter, Cameron and Boonsobhak, 2006), adaptive neuromorphic olfaction chip(Koickal, Hamilton, Tan, Covington, Gardner and Pearce, 2007), effect of process mismatch(Cameron, Murray and Boonsobhak, 2007) and floating gate learning array with STDP(Pankaala, Laiho and Hasler, 2009) is suggested. Or again, using digital circuits, navigation robot(Arena, Fortuna, Frasca, Patane and Sala, 2007) and auditory system based on FPGA(Cassidy, Denham, Kanold and Andreou, 2007) is shown. Furthermore, mixed signal circuits with STDP (Schemmel, Grubl, Meier and Mueller, 2006) are proposed. However, these models require

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either complex cell body circuits or large scale circuits. Moreover, most of circuits use only one time window in STDP, or use several circuits with two time windows in STDP, respectively.

We previously proposed a simple cell body circuit of a pulse-type hardware neuron model (P-HNM) using CMOS that approximately simulates pulse signals as the means of information transmission in the brain (Sekine, Sumiyama, Saeki and Aihara, 2001, Saeki, Sekine, and Aihara, 1999). And so, we proposed an asymmetric type of STDP hardware model. Moreover, we studied the robustness of this circuit. As a result, we showed that it was able to make IC implementation (Saeki, Hayashi and Sekine, 2006, Saeki, Hayashi and Sekine, 2008, Shimizu, Saeki and Sekine, 2009)

In this paper, we use simple cell body pulse-type neuro devices, and we propose a synaptic weight generation circuit with two time windows in STDP. As to its application, we study the storage of temporal sequence patterns.

2 PULSE-TYPE NEURO DEVICES WITH STDP

An STDP block diagram is shown in Fig. 1. This block diagram has cell body blocks and an STDP block. When pulses are inputted to each temporal summation block, output pulses from each temporal summation block have first-order delays and are transmitted to the subsequent blocks. When the post-synaptic cell generates the pulses, the synaptic weight W_p between pre- and post-synaptic cells is reinforced based on the output amplitude of the temporal summation block with the pre-synaptic cell. On the other hand, when the pre-synaptic cell generates the pulses, W_p is suppressed based on the output amplitude of the temporal summation block with the post-synaptic cell.

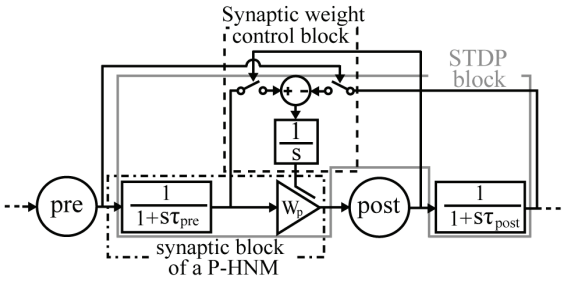
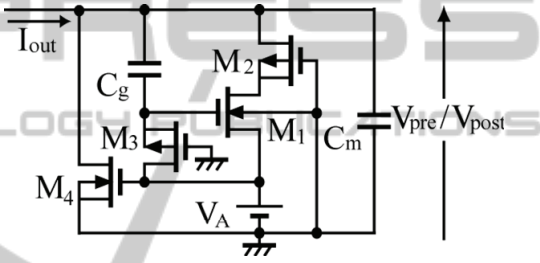


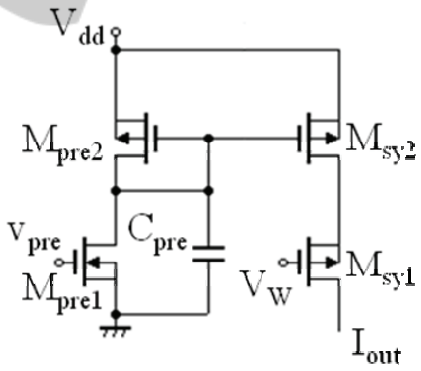
Figure 1: STDP block diagram.

2.1 Circuits of Pulse-Type Neuro Devices

A pulse-type neuro device is shown in Fig. 2. The pulse-type neuro device consists of a cell body circuit and a synaptic circuit. Figure (a) shows the cell body circuit. When I_{out} is inputted to the cell body circuit, output pulses are generated. This circuit has a threshold and a refractory period characteristic. Figure (b) shows the synaptic circuit. When pulses are inputted to the input terminal V_{pre} of the synaptic circuit from the pre-synaptic cell, I_{out} is generated. The current I_{out} changes according to V_w. Therefore, the synaptic weight between the pre- and post-synaptic cells can be controlled by V_w. Spatial summation circuits can also be constructed when a series circuit of M_{sy1} and M_{sy2} is connected in parallel.



(a) Cell body circuit



(b) Synaptic circuit

Figure 2: Pulse-type neuro device.

2.2 Synaptic Weight Generation Circuit

It is reported that the two time windows in STDP depends on the influence of an inhibitory neuron (Tsukada, Aihara, Kobayashi and Shimazaki, 2005). Focusing on this biological report, we investigated the synaptic weight generation circuit that is able to change two time windows by changing voltages.

Figure 3 shows the details of the synaptic weight control block in Fig. 1. This circuit consists in part

of five blocks; three temporal summation blocks (D_{pre}, D_{post} and D_i) including first-order-delay elements, a sampling block and an integral block. Switch S_1 is assumed depending on stimuli of inhibitory neuron. v_{pre} and v_{post} display output voltages of pre-synaptic cell and post-synaptic cell, respectively. The voltage V_w is the output voltage of this circuit and is the parameter that controls the synaptic weight between the pre- and post-synaptic cells.

The synaptic weight generation circuit is shown in Fig. 4. This proposed circuit shows that the two time windows depend on the V_i. C_w represents the integral block. $Mpre_6$, $Mpost_4$ and M_{i4} are sampling blocks. D_{pre}, D_{post} and D_i have first-order delay elements. Furthermore, M_{pre2} to M_{pre3}, M_{pre4} to M_{pre5}, M_{post2} to M_{post3}, M_{i2} to M_{i3} are constructed by current mirror connection. V_i is inputted to the input terminal of the MOS switch consist of M_a and M_b. If V_i is threshold voltage or over, D_i is not used. On the other hand, if V_i is threshold voltage or under, D_i is used. That is to say, it is able to control first-order-delay elements.

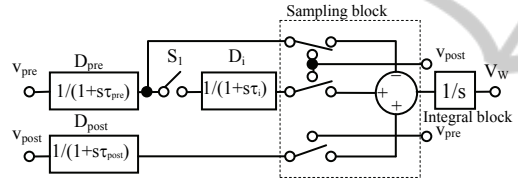


Figure 3: Syanptic weight control block.

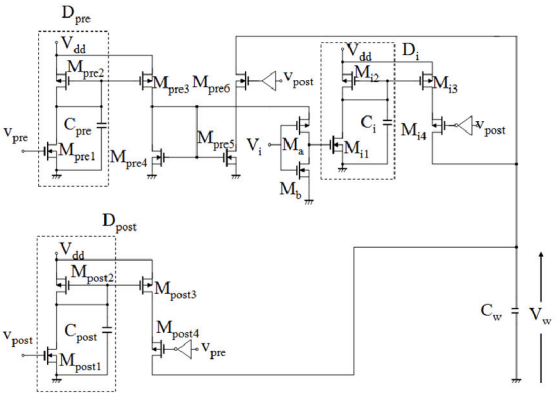
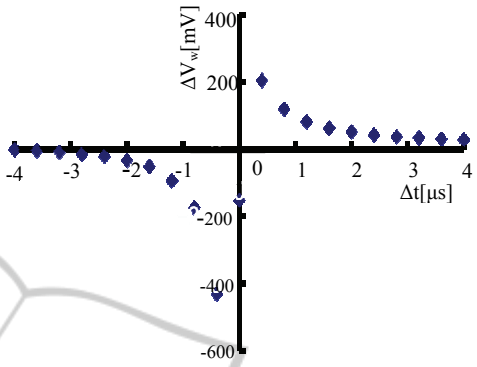
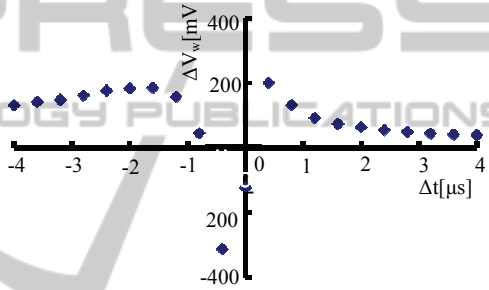


Figure 4: Synaptic weight generation circuit.

A function of V_w in the synaptic weight generation circuit is shown in Fig. 5. The horizontal axis is the time interval Δt, which is the time of the pre-synaptic pulse minus the time of the post-synaptic pulse, and the vertical axis is the amount of voltage change ΔV_w. Figure (a) displays an asymmetric time window, when V_i is 3[V] in proposed synaptic weight generation circuit. Figure (b) displays a symmetric time window, when V_i is -3[V] in proposed synaptic weight generation circuit. Therefore, it is shown that two time windows in STDP are obtained by changing voltage V_i.



(a) Asymmetric time window.



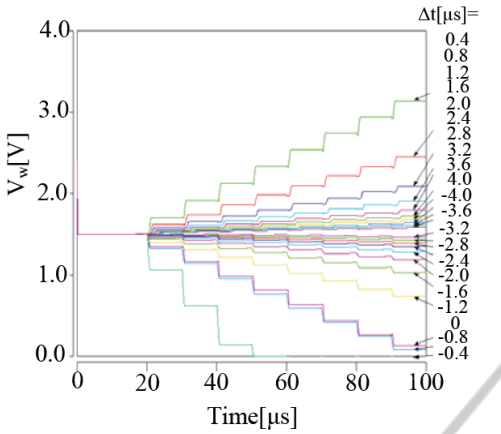
(b) Symmetric time window.

Figure 5: Characteristics of V_w in the synaptic weight.

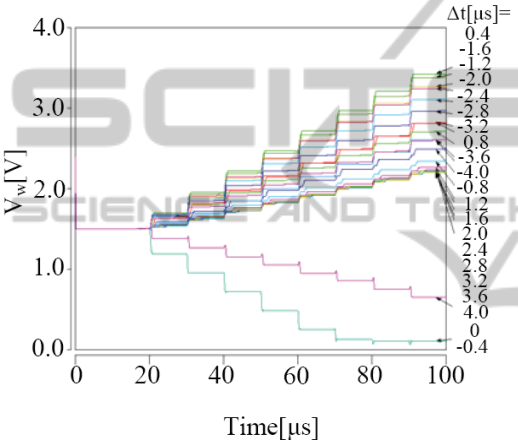
Figure 6 shows the simulation result for the synaptic weight changes by the STDP function. (a) and (b) show the asymmetric and the symmetric time window type, respectively. Δt is the parameter.

3 MEMORY OF TEMPORAL SEQUENCES PATTERNS

Figure 7 shows a construction of a hardware STDP model. It shows a Hopfield-type network which is the interactive connection for all neuron models. In this figure, cell A ~ J are cell body models, the open circles indicate STDP synapses. Input cells A ~ J show the input stimulus current. If we assume that cell A = $cell_{pre}$ and cell B = $cell_{post}$, the synaptic weight displayed will be $W_{A,B}$ (cell A to cell B) and $W_{B,A}$ (cell B to cell A). Furthermore, $W_{A,B}$ and $W_{B,A}$ are changed depending on the output pulse timing from cell A and cell B. That is to say, temporal



(a) Time transition in asymmetric time window.



(b) Time transition in symmetric time window.

Figure 6: Time transition in synaptic weight.

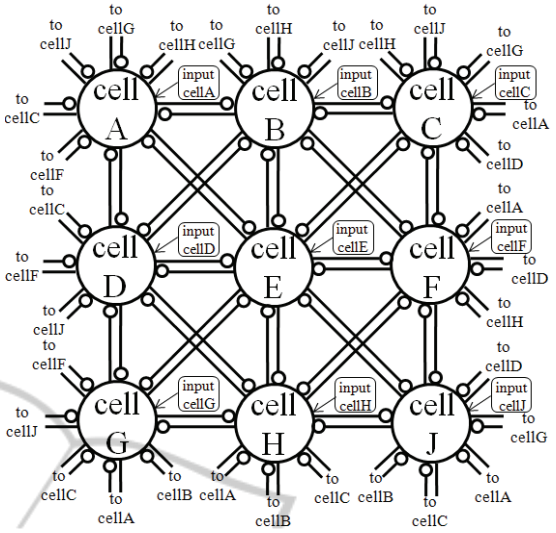


Figure 7: Construction of hardware STDP model.

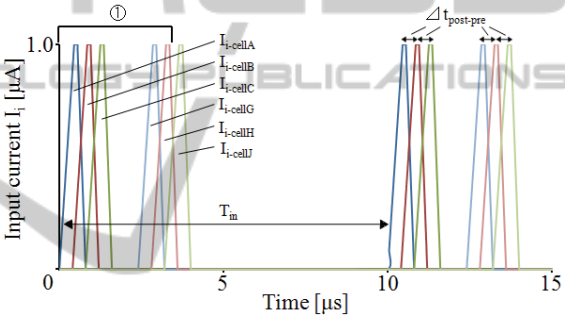


Figure 8: Example of current patterns of temporal sequence pulses.

sequence patterns are stored by using synaptic weight, which is dependent on the differential pulse timing. In this examination, we use the nine pulse-type neuro devices with STDP cells A ~ J.

Figure 8 shows an example of the current patterns of the temporal sequence pulses for ① which are input to $cell_{pre}$ and $cell_{post}$. The horizontal axis corresponds to time, while the vertical axis shows the input current for each pulse-type neuro device. Here, Δt is the interval, which is the time difference between the post-synaptic and pre-synaptic pulses, and T_{in} is the period of the pulse current. So, Δt = 0.4 μs and T_{in} = 10 μs are used as an example. Here, there is no input for the pulse current when we assume that cell D, E, and F have no input. The current patterns of the temporal sequence pulses after input are shown as ①.

Figure 9 shows a distribution of synaptic-weight. The horizontal axis corresponds to the $cell_{pre}$, while the vertical axis shows the $cell_{post}$. This result shows when V_i is 3[V] and -3[V] in the proposed synaptic weight generation circuit. V_w/V_{MAX} represent output voltage V_w of the synaptic weight generation circuit that is normalized with V_{MAX}(= V_{dd}). The black squares mean that $W_{pre,post}$ is strong when V_w/V_{MAX} approaches 0.0. On the other hand, the white squares mean that $W_{pre,post}$ is weak when V_w/V_{MAX} approaches 1.0. That is to say, it is shown that the synaptic weight changes depending on the input current patterns of temporal sequence pulses.

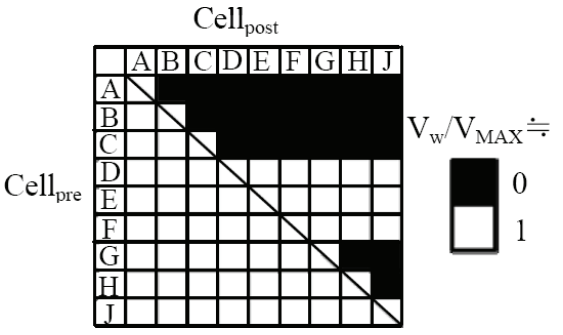


Figure 9: Distribution of synaptic-weight.

Figure 10 shows an example of the order of the pulses that the pulse-type neuro device uses at each cell output. The horizontal axis corresponds to time, while the vertical axis shows the output voltage of each pulse-type neuro device. This result shows that the order of the output pulses that the pulse-type neuro device with two time windows in STDP uses for each cell output is dependent on each of the synaptic weights shown in Fig. 9. This is similar to the order of the current patterns of the temporal sequence pulses in ①. Therefore, we showed that the pulse-type neuro device with STDP stores the temporal sequence output voltage patterns which obey the temporal sequence input current patterns.

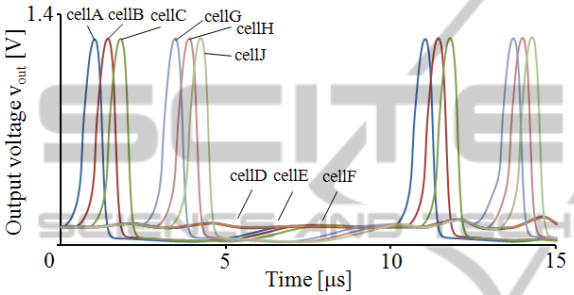


Figure 10: Output waveforms of pulse-type neuro device with STDP.

4 CONCLUSIONS

For purpose of constructing brain-type information processing systems, we constructed neuro devices with learning functions.

In this paper, we focus on two time windows in STDP, and we propose a synaptic weight generation circuit which indicates an asymmetric or a symmetric time window by changing voltages in the proposed circuit.

As a result, we show that a pulse-type neuro device with two time windows in STDP stores temporal sequence output voltage patterns which conform to the temporal sequence input current patterns for memory, because synaptic weight changes depending on the input current patterns of temporal sequence pulses. From this result, it is shown that there is every possibility of constructing an associative memory device which includes autoassociative and heteroassociative memory using the two time windows.

In the future, we will study the recall of two the states (autoassociative and heteroassociative) of temporal sequence patterns using a pulse-type neuro device with two time windows in STDP.

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