ANALYSIS AND DESIGN OF COMPUTER ARCHITECTURE CIRCUITS WITH CONTROLLABLE DELAY LINE

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Abstract: In this work classical and modern control theory methods are applied for rigorous mathematical analysis and design of different computer architecture circuits such as clock generators, synchronization systems and others. The present work is devoted to the questions of analysis and synthesis of feedback systems, in which there are controllable delay lines. In the work it is mathematically strictly shown that *RC*-chain can be used as a controllable delay line for different problems of circuit engineering if the chain is sequentially connected with hysteretic relay. This relay is either artificially introduced or shows itself as non-ideality of logic elements. The possibility of phase-locked loop application for time delay control is considered.

1 INTRODUCTION

The work is devoted to the questions of analysis and synthesis of feedback systems, in which there are controllable delay lines. First of all this is a class of controllable clock generators and clocked circuits, which perform the functions of summators (Cormen et al., 1990).

In clocked circuits it is necessary that the delay was by the one tact. For this purpose we need in a special setting of parameters of delay lines, which will be described in details. The generators, constructed on logic elements and delay lines, are not high-stable with respect to frequency (Ugrumov, 2000). Therefore, for their stabilization and synchronization by phase-locked loops it is necessary to introduce a controllable parameter in delay line. A class of such delay lines, the block-scheme of which is shown in Fig. 1, is considered.

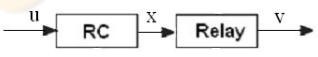

Figure 1: Delay line.

The *RC*-chains are often used in circuit engineering as delay lines (Ugrumov, 2000). We assume that the relation between the input u and the output x is described by the following standard equation of *RC*-chain

$$RC\frac{dx}{dt} + x = u(t), \qquad (1)$$

where R is a resistance, C is a circuit capacitance.

The relation between the input x and the output v is described by the graph of "relay with hysteresis"function, which is shown in Fig. 2. Here μ_1 and μ_2

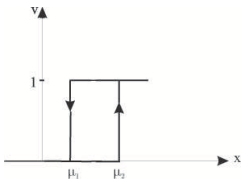

Figure 2: Relay with hysteresis.

are certain numbers from the interval $(0,1)$. The theory and practice of application of such relay blocks in feedback systems is well described in (Popov, 1979; Krasnosel'skii and Pokrovskii, 1983).

In the present work we consider only the functions $u(t)$, which takes the values either 0 or 1 on certain intervals. Therefore, the solutions $x(t)$ of equation (1) are continuous, piecewise-differentiable and

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piecewise-monotone functions. It follows that the graph in Fig. 2 correctly defines the output $v(t)$. Further it will be shown that the hysteretic effect is of great importance for synthesis both of clock generators and of clocked summators. This effect always occurs in real (non-ideal) logic elements. Since the output of delay line is often the input of logic element, it is convenient to connect such hysteretic effect with *RC*-chain and to consider it in the frame of block-scheme in Fig. 1. In some cases for improvement of a quality of delay line operation it is possible to introduce additional block "relay with hysteresis", which provides a required delay time and stability of system operation.

We can show here the analogy with a classical study of Watt's regulator by I.A.Vyshnegradskii (Andronov and Voznesenskii, 1949; Leonov, 2001). Recall a main conclusion of Vyshnegradskii: "without friction the regulator is lacking". But if a friction "is not sufficient", then it is possible to introduce a special correcting device, dashpot, which provides a stable operation of system. In the case now being considered the friction is replaced by hysteretic effect and the above classical scheme of reasoning is repeated. This becomes especially clear if we consider the synthesis of clock generators.

For clocked summators it turns out rational the introduction of two-stage delay lines, which shift a unit impulse for the one tact. The latter permits us to use a three-bit summator for any summation, confining our attention to a minimal number of circuit elements.

The application of methods and technique of the classical control theory (Burkin et al., 1996; Leonov et al., 1996, Popov, 1979; Krasnosel'skii and Pokrovskii, 1983; Andronov and Voznesenskii, 1949) permits us to find the solution of considered problems, applying very simple mathematical constructions.

2 DELAY LINES FOR SYNTHESIS OF CONTROLLABLE CLOCK GENERATORS

Consider the block-scheme in Fig. 3 and, recall the

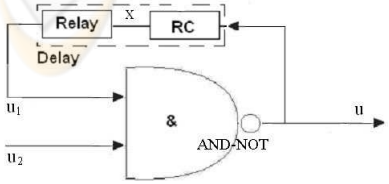

Figure 3: Clock generator on Block AND-NOT and delay line.

table for Block AND-NOT output

u_1	u_2	u
0	0	1
0	1	1
1	0	1
1	1	0

Truth table of Block AND – NOT

Let $u_2(t) = 0$ for $t < T$, $T > 0$. Then $u(t) = 1$ for $t < T$ and at the input $x(t)$ there occurs (after a transient process) the signal $x(t) = 1$. Suppose, $x(t) = 1$ on $[0,T]$. Then $u_1(t) = 1$ on $[0,T]$ and a system is in equilibrium:

$$1 = u_1(t) = x(t) = u(t), \quad u_2(t) = 0.$$

The inclusion of clock generator is realized by the change of u_2 from the state 0 to the state 1: $u_2(t) = 1$, $\forall t > T$. Then on the certain interval (T, T_1) we have $u(t) = 0$. This implies that $u_1(t) = 1$ for $t \in (T, T_1)$, where

$$T_1 = T + RC \ln \frac{1}{\mu_1} \tag{2}$$

and $u_1(t) = 0$ on a certain interval (T_1, T_2).

Really, from equation (1) it follows that on (T, T_1) we have $x(t) = e^{-\alpha t}$, $\alpha = 1/RC$. In this case $u_1(t) = 1$ for $t \in (T, T_1)$, where T_1 is from relation (2), and $u_1(t) = 0$ for $t \in (T_1, T_2)$, where T_2 will be determined below. From the latter relation it should be that $u(t) = 1$ for $t \in (T_1, T_2)$. This implies the following relation

$$T_2 = T_1 + RC \ln \tfrac{1-\mu_1}{1-\mu_2}, \quad x(T_2) = \mu_2.$$

In the case when $\mu_1 = 1 - \mu_2$, $\mu_2 \in (1/2, 1)$, we obtain

$$\tau = T_1 - T_0 = T_2 - T_1 = RC \ln \tfrac{\mu_2}{1-\mu_2},$$
$$T_0 = T + RC \ln \tfrac{1}{\mu_2},$$

and 2τ-periodic sequence at the output u:

$$u(t) = 0, \quad \forall t \in [T_0, T_0 + \tau),$$
$$u(t) = 1, \quad \forall t \in [T_0 + \tau, T_0 + 2\tau).$$

Thus, the block-scheme in Fig. 3 is a clock generator with the frequency

$$\omega = \frac{1}{2\tau} = \left(2R \ln \frac{\mu_2}{1-\mu_2}\right)^{-1} C^{-1}. \tag{3}$$

We compare this frequency with the frequency of harmonic *LC*-oscillator:

$$\omega = 1/\sqrt{LC} \tag{4}$$

At present it is developed different methods of control of a frequency of harmonic oscillators by means of a slow (with respect to the high frequency ω) change of parameter C. It is especially widely extended the phase-locked loops (Viterbi, 1966; Lindsey, 1972). In the past decade similar constructions are actively developed and applied to the clock generators with frequency (3) (Solonina et al., 2000).

3 DELAY LINES FOR CLOCK IMPULSES

Consider the delay line, the block-scheme of which is shown in Fig. 1. Let $u(t)$ be 2τ-periodic sequence of impulses:

$$u(t)=0, \forall t\in[0,\tau),\ u(t)=1, \forall t\in[\tau,2\tau). \qquad (5)$$

If we choose the initial data $x(0,x_0)=x_0$ so that the relation

$$\tau = RC\ln\frac{x_0}{1-x_0},\quad x_0\in(1/2,1), \qquad (6)$$

is satisfied, then $x(\tau,x_0)=1-x_0,\quad x(2\tau,x_0)=x_0$. In this case the graph of 2τ-periodic function $x(t)$ is shown in Fig. 4.

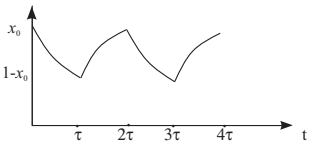

Figure 4: Periodic output of RC-chain.

It is well known (Leonov, 2001) that for all other solutions of equation (1) $x(t,y_0)$ the following relation

$$\lim_{t\to+\infty}(x(t,x_0)-x(t,y_0))=0 \qquad (7)$$

is satisfied. If we choose $x_0>\mu_2,\ 1-x_0<\mu_1$, then relation (7) implies that after transient process, at the output v (of delay line) we obtain 2τ-periodic sequence of impulses:

$$\begin{aligned} &v(t)=0,\ \forall t\in\left[RC\ln\tfrac{x_0}{\mu_1},\tau+RC\ln\tfrac{x_0}{1-\mu_2}\right),\\ &v(t)=1,\ \forall t\in\left[\tau+RC\ln\tfrac{x_0}{1-\mu_2},2\tau+RC\ln\tfrac{x_0}{\mu_1}\right). \end{aligned} \qquad (8)$$

Note that for $\mu_1=1-x_0+\varepsilon,\ \mu_2=x_0-\varepsilon$, where $\varepsilon>0$ is a small parameter, from (8) we have

$$\begin{aligned} &v(t)=0,\quad \forall t\in[\tau_\varepsilon,\tau+\tau_\varepsilon),\\ &v(t)=1,\quad \forall t\in[\tau+\tau_\varepsilon,2\tau+\tau_\varepsilon), \end{aligned} \qquad (9)$$

where

$$\tau_\varepsilon = RC\ln\left(\frac{x_0}{1-x_0+\varepsilon}\right)\xrightarrow[\varepsilon\to0]{}\tau. \qquad (10)$$

Recall that $x_0\in(1/2,1)$ and τ is determined from relation (6).

Thus, the block-scheme in Fig. 1 realizes asymptotically the time delay τ: after transient process (see relation (7)) at the output v we observe relation (9), in which case relation (10) is satisfied.

Consider now a certain extension of the above case. Let $u(t)$ be a certain sequence of clock impulses (not necessarily 2τ-periodic) such that

$$u(t)=0,\quad \forall t\in[2k\tau,(2k+1)\tau),\ k=0,1,\ldots$$

and on each of intervals $((2k+1)\tau,2k+2)\tau)$ it can take the value either 0 or 1.

Now we consider the case when the delay line operates in working conditions after transient process. In this case, taking into account the above reasoning, we can assume that for the certain fixed k there occur the following restrictions:

$$\begin{aligned} &u(t)=1,\quad \forall t\in[(2k+1)\tau,2(k+1)\tau)\\ &x((2k+1)\tau)\in(0,1-x_0), \end{aligned}$$

where x_0 satisfies relation (6).

We shall show that in this case it can be made such a choice of parameters of delay line, for which asymptotically (at $\varepsilon\to0$) the delay time of unit impulse is τ. For this purpose we can take the obvious inequalities

$$\begin{aligned} &x(t,(2k+1)\tau,0)\le x(t,(2k+1)\tau,x((2k+1)\tau)\le\\ &\le x(t,(2k+1)\tau,1-x_0),\quad \forall t\ge(2k+1)\tau. \end{aligned}$$

Here $x((2k+1)\tau,(2k+1)\tau,y_0)=y_0$. By the previous relations $\mu_1=1-x_0+\varepsilon,\ \mu_2=x_0-\varepsilon$ we obtain

$$\begin{aligned} &v(t)=0,\ \forall t\in((2k+1)\tau,(2k+1)\tau+\tau_\varepsilon),\\ &v(t)=1,\ \forall t\in((2k+1)\tau+\widetilde{\tau}_\varepsilon,(2k+1)\tau+\tau_\varepsilon+\widetilde{\widetilde{\tau}}_\varepsilon). \end{aligned}$$

Here

$$\widetilde{\tau}_\varepsilon = RC\ln(\frac{1}{1-x_0+\varepsilon}),\widetilde{\widetilde{\tau}}_\varepsilon = RC\ln(\frac{x_0-\varepsilon}{1-x_0+\varepsilon}).$$

Choosing $x_0=1-\sqrt{\varepsilon}$, we obtain the following formulas for parameters of delay line, which shifts unit impulse with accuracy up to $\sqrt{\varepsilon}$ for time τ:

$$\mu_1=\sqrt{\varepsilon}+\varepsilon,\mu_2=1-\mu_1,RC=\tau/\ln\frac{1}{\sqrt{\varepsilon}}. \qquad (11)$$

This implies that for the asymptotical shift of unit impulse for time 2τ it is necessary to apply two-stage delay line with parameters (11) (Fig. 5). We proceed

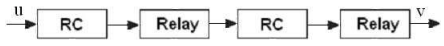

Figure 5: Two-stage delay line.

now to the clocked circuits for bit summation (Cormen et al., 1990) (Fig. 6). Here Σ is a standard sum-

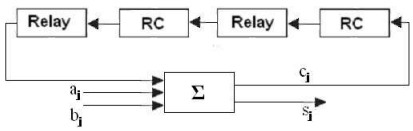

Figure 6: Clocked summator.

mator, at the input of which we have three bits, $c_0=0$. As the delay line we can use a two-stage delay line with parameters (11) (Fig. 5). The time between the

arrival of the signals a_j and a_{j+1} (and also b_j and b_{j+1}) is equal to τ. It is easily seen that the output $s_k s_{k-1} \dots s_0$ is a sum of two numbers $a_{k-1}a_{k-2}\dots a_0$ and $b_{k-1}b_{k-2}\dots b_0$. Thus, the delay line considered permits us to construct the summators with minimal number of circuit elements.

4 CONCLUSIONS

In the present work it is mathematically rigorously shown that *RC*-chain can be used as a controllable delay line for different problems of circuit engineering if the chain is sequentially connected with hysteretic relay. This relay is either artificially introduced or shows itself as non-ideality of logic elements.

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