# EXPERIMENTAL DIGITAL BPSK MODULATOR DESIGN WITH VHDL CODE FOR BIODEVICES APPLICATIONS

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Abstract: In this paper, we propose a new simple design for a BPSK modulator applied to implant telemetry applications as demonstrated. We used hardware description language VHDL (IEEE standard) to generate a BPSK digital signal. The carrier and data are interfaced to the CPLD and FPGAs board for testing, we used the local clock oscillator, which is operating at 25.175 MHz reduced into 12.5 MHz for the carrier and 2Mbps for data source. The modelled modulator has been designed simulated and performance was evaluated by measurements, considering low power consumption and size for medical purpose. Moreover, the advantages of this modulator are it can be reconfigured and upgraded to enhance the bit rate.

## 1 INTRODUCTION

Wireless infrastructure is fast growing and this technology may also be used for medical applications such as biotelemetry, telemedicine and healthcare (R.Harrison, et al., 2006). One of these applications is transcutaneous wireless implant telemetry, in order to communicate through wireless inductive coupling to transfer the power and data to a battery less implant (K.D.Wiseet al, 2004; C.Sauer et al, 2004). Demand for higher data rates is high as a result of increasing the electrode numbers for reading nerve signal information or controlling data. In such applications BPSK has advantages over ASK and FSK modulations. The advantage of BPSK is having fixed carrier signal amplitude that provides stable power transfer and independent data modulation. This is suitable to provide a constant RF signal into an implant device. The advantage is high readability for DC voltage supply at different distances between reader coils and implant part. We propose in this work to develop VHDL code to generate a digital BPSK signal for improving modulator performance and increasing the data rate (Bob Zeidman, 2002). Compared to the other analogue modulators, this type of modulator provides digital synthesis and the flexibility to reconfigure and upgrade with the two most often used languages VHDL-and Verilog- based (P.Niktin, et al., 2005; J.S. Ruque, et al., 2005).

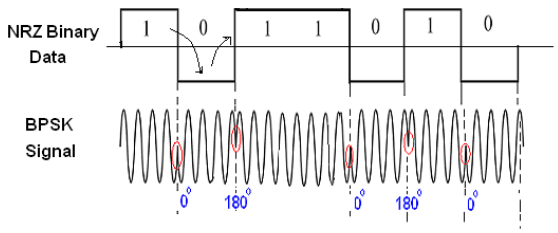
## 2 METHOD

The BPSK signal can be represented mathematically in an analogue way as in equation (1).

$$S_{BPSK}(t) = m(t)\sqrt{\frac{2E_b}{T_b}}Cos(w_{rf}t + \phi_{rf}) \qquad (1)$$

As demonstrated in Figure 1, for this technique it is essential to convert the binary data $m(t)$ into a NRZ signal that maps a logic '0' to -1V(nominal) and logic '1' to +1V. This data signal controls the transition shift $(0, \pi)$ for the carrier signal. This results in high power consumption for these types of analogue modulators, reduces their efficiency and limits their biomedical application. This also increases the hardware complexity of the circuit and produces a large physical device.

The proposed modulator is developed with VHDL description code to generate carrier shifter




Figures 1: Illustrated the BPSK waveform with respect NRZ) data transitions.



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frequencies (0, 180°) which are controlled by the input binary data to perform the transition of the BPSK signal (I. Grout, et al, 2005). The modulator consists of digital and analogue parts as depicted in Figure 2. The output is selected by the multiplexer then filtered with a passive Band Pass Filter (BPF) to eliminate the higher frequencies and the harmonics associated with the square wave signal in order to provide the transmit analogue signal (Tx).

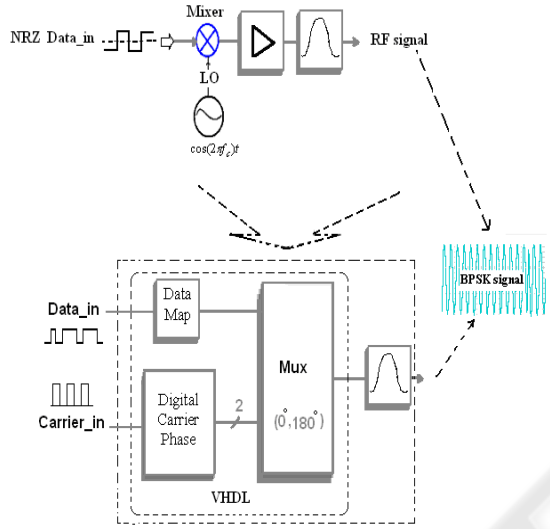


Figure 2: Illustration of the block diagram for the proposed BPSK Modulator.

The simulated random data signal (Data_in) that is generated by a PN sequence can be represented by Fourier series analysis as in equation (2).

$$PN(t) = \sum_{n=-\infty}^{\infty} c_n p(t - nT_c) \quad (2)$$

Where the input carrier signal is a periodic pulse train signal and mathematically expressed by the Fourier series as in equation (3).

$$Carrier(t) = \frac{4}{\pi} \sum_{k=1}^{\infty} \frac{\sin((2k-1)w_c t)}{(2k-1)} \quad (3)$$

The filter is essential for the modulator to complete the process (off-chip). The output signal produced by it is an analogue form. We investigated two types of filters in this paper, Low Pass Filter (LPF) and Band Pass Filter (BPF). The BPSK VHDL output signal is fed into the test filters. These filter it to pass the fundamental frequency ( $f \pm data$ ) and to remove the harmonics and the DC component. Our prototype analogue filter uses the Chebyshev filter II as opposed to the other filters such as Chebyshev I, Butterworth, Elliptic and Bessel. Our second choice is Butterworth LPF as this was observed to give better performance than the other types.

## 3 MODULE SIMULATION

### *A. Simulink/ MATLAB Simulation*

The BPSK modulator was designed and simulated with Simulink/MATLAB to verify and validate the modulator specifications. The demodulator is also constructed using the same tools to examine the performance of the proposed modulator. The architecture block diagram of Tx_Mod is shown in

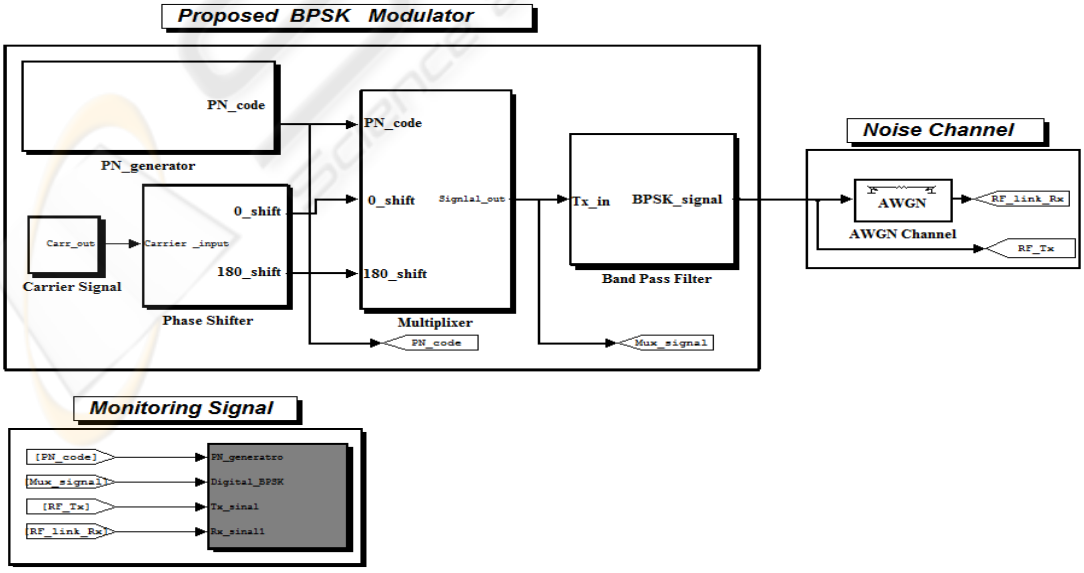


Figure 3: The simulink BSPK modulator diagram.

Figure 3. The simulation result of the Simulink modulator is presented in Figure 4. The signal in Figure 4a presents the digital BPSK signal while the signal in Figure 4b presents the filtered BPSK output of the BPF. The Tx and the Rx data are presented in Figure 4c and Figure 4d respectively. Figure 5 shows the spectrum of the transmitted RF signal (CH1) and the received RF signal (CH2) in the presence of noise (AWGN). Finally Figure 6 shows the simulation result for the Bit Error Rate (BER) of the designed demodulator.

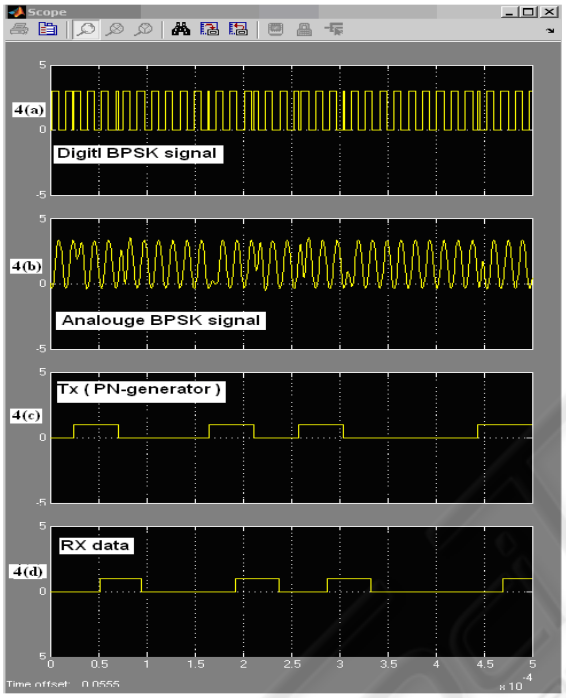


Figure 4: The simulated BPSK modulator output signals results by Matlab/Simulink at frequency12.5 MHz.

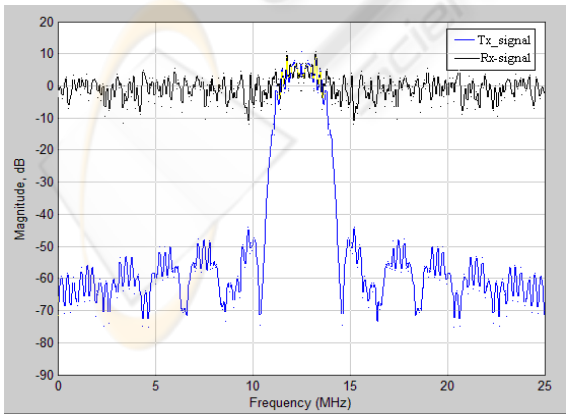


Figure 5: The Spectrum of BPSK transmit and receive signals at Data rate 2MHz, carrier 12.5MHz.

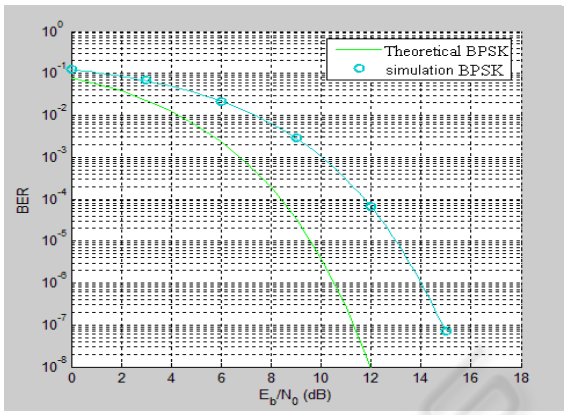


Figure 6: The BER simulation diagram of demodulator signal from the proposed BPSK modulator.

*B. VHDL-code Simulation*

The modulator is implemented using VHDL code and built by the Altera UP2 development kit board. The carrier frequency 12.5 MHz was generated by the local clock signal that operates at 25.175 MHz. The signal data clock was reduced to 2MHz by a frequency divider then used to generate a random PN_sequence, which provided the transitions of the carrier selected by the multiplexer (V.Pwdroni, 2007). The behavioural block diagram of the VHDL code of the BPSK modulator is illustrated in Figure_7, whilst the simulated result of this modulator is presented in Figure 8 which demonstrates the output signal waveforms indicating the transitions (0°,180°) of the carrier signal (output of multiplexer) due to the data source.

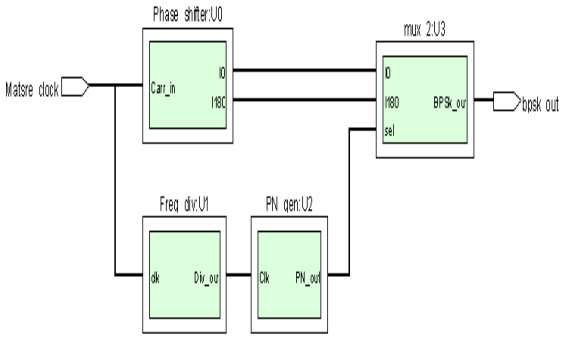


Figure 7: The VHDL Digital BPSK Modulator.

# 4 EXPERIMENTAL RESULTS AND DISCUSSION

In this section we provide the measurements which were conducted using the Altera UP2 Development

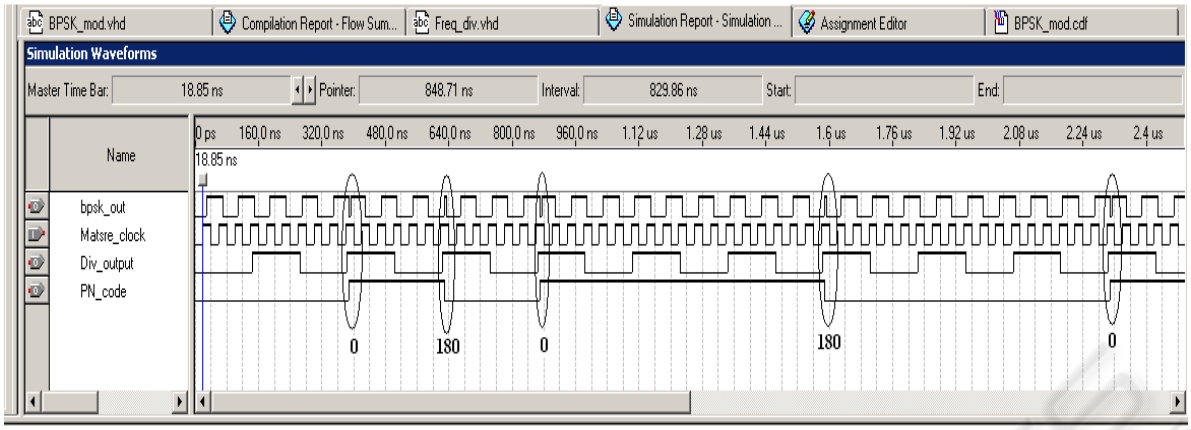


Figure 8: The simulated waveform generated by Altera development tools for BPSK Modulator.

kit board for testing the VHDL code modulator and comparing the performance with the simulated BPSK modulation. The Agilent digital demodulator (E8048A VXI) is used to receive the filtered RF BPSK signal, and analyse the parameters of the transmitted BPSK signal Tx as demonstrated in Figure 9.

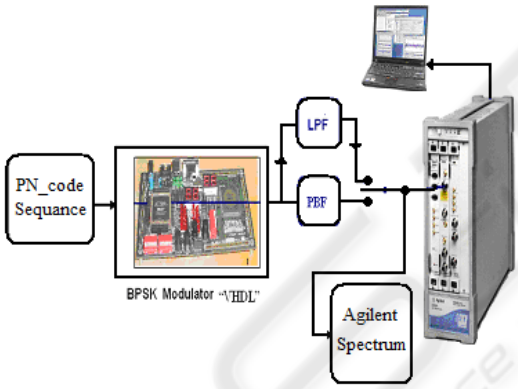


Figure 9: Illustrated the Lab measurement withUK2 Alter.

Aboard and Agilent digital demodulator (E8048A)The desired carrier signal was generated from the master clock on the circuit board that operates at 25.175 MHz, and the carrier phase acquires two discrete states (0, π) at frequency 12.5 MHz. This corresponds to the PN-code data source generated with VHDL code inside the FPGAs at 2Mbps in order to produce the BPSK modulation. The behavioural simulation results produced BPSK digital signal, passed through passive BPF for harmonics separation. We investigated two prototypes of filters in this paper, LPF and BPF.

Our choice was the Chebyshev filter II as this has better performance than the other types. The filtered output signals, captured with Tektronix scope and Agilent spectrum analyser are demonstrated in Figures 10 and 11 respectively.

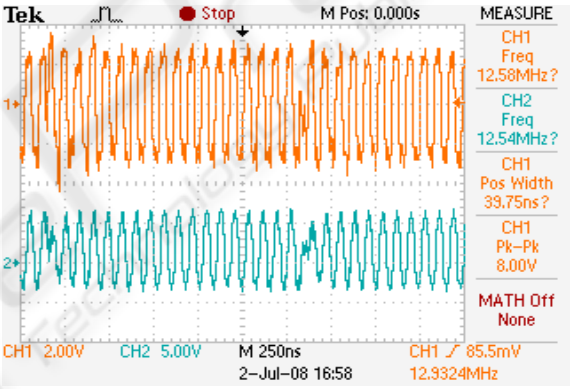


Figure 10: The output of VHDL BPSK modulator (digital signal) Top and filtered signal bottom at carrier frequency 12.5 MHz.

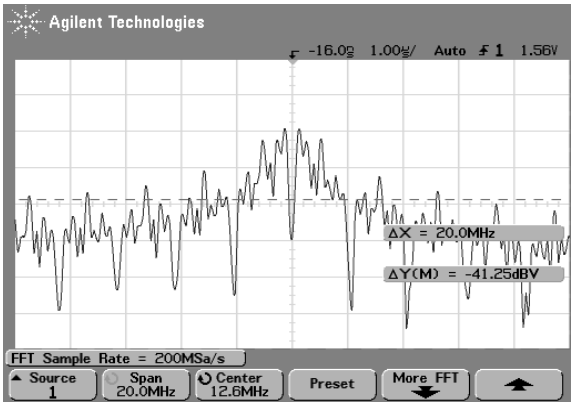


Figure 11: The Spectrum of BPSK transmitted signal at carrier 12.5 MHz.

The Agilent digital demodulator was used to measure the spectrum of the Rx BPSK signal as

shown in Figure 12 while the constellation diagram of the demodulated signal is presented in Figure 13.

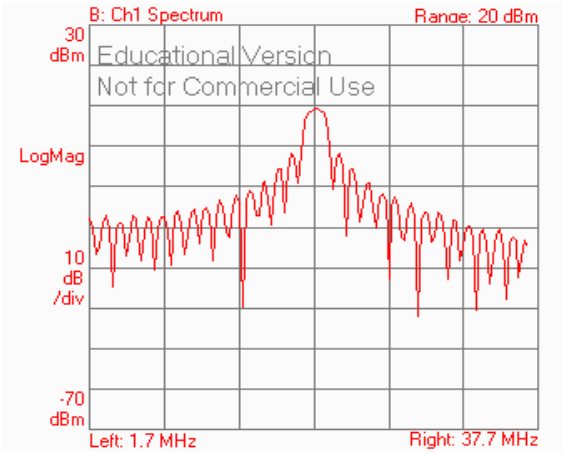


Figure 12: The Rx- BPSK signal spectrum at 12.5 MHz carrier (data rate 2Mbps).

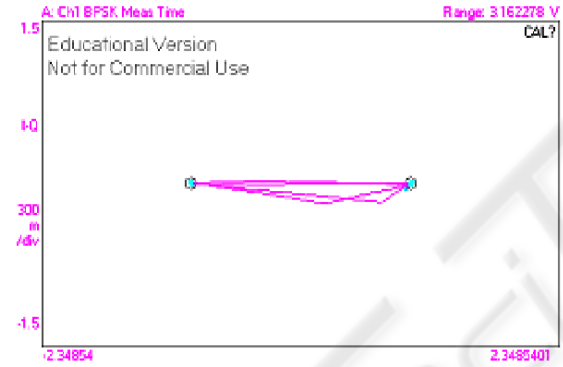


Figure 13: The constellation diagram of BPSK at Demodulator using Agilent digital demodulator (E8048A).

## 5 CONCLUSIONS

We implemented a new simple BPSK digital modulator model in the Simulink MATLAB environment. This has been successfully implemented using hardware description language VHDL code by the Altera UP2 development board. The modulator generates the BPSK signal directly from the binary data in order to control the carrier signal. The output producing a modulated digital signal was filtered to transmit through a miniature BPF. Experimentally measurements are presented at carrier frequency 12.50 MHz, and data rate 2Mbps, which present good performance with high data rate and carrier suppression >35dB. The filter is a critical part of the design. For this work we designed and simulated different types of analogue filter and compared them to choose the best filter performance. The simulation results were that the Chebyshev I & II, appeared optimum at BPFs compared to the others, and optimum LPF performance was form the Butterworth type. Digital filters could be implemented to allow integration with the digital modulator device. However the disadvantage of digital filter is that they need clocking at high multiples of the sampling frequency which increases the power consumption and size. As future work, it is still necessary to investigate other methods to improve the harmonic rejection performance of the analogue output filters by digital synthesis of alternative waveforms at the modulator. It is also an intention to up-convert the signal into an ISM unlicensed frequency band (e.g. 402~405 MHz) for biomedical telemetry purposes.

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