Mature 25Gb/s Silicon Photonic Platform towards Multi-Layer Circuits for High Integration Level Aplications

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Abstract: Silicon photonics is definitely a key technology in next-generation communication systems from Long-Haul networks to short reach data interconnects. To address 25 Gb/s and above applications, we present our R&D platform that uses a CMOS foundry line. The fabrication process is following a modular integration scheme which leads to a flexible platform, allowing various device combinations. Moreover this platform is associated to a device library in a PDK which includes specific photonic features and which is compatible with commercial EDA tools. Based on the maturity of this platform to build high-speed optical transceivers, we present our strategy to anticipate the next integration disruptive level by implementing multi-layer photonic circuits. Such a technology represents a new paradigm for the design of very high integration circuits that we consider first for optical interposer, and finally for optical network on chip with the convergence of photonics and electronics.

1 INTRODUCTION

Optical communications are definitively playing a major role in high speed interconnects in servers, datacenters, and supercomputers. In these systems, copper cables have been replaced by active optical cables in order to deal with data rate typically above 100Gbps per module. Mainly based today on optical sub-assembly modules using VCSEL emitters, optical links remain an expensive solution. As a result, the next generation of optical components must meet the challenge of high speed, low cost, low energy consumption, and high–volume manufacturing. Silicon photonics is now widely accepted as a key technology (Kopp, 2011) to cope with this challenge, leading also to a convergence between photonics and electronics in terms of fabrication foundry, design tool environment, and circuit co-integration.

In this paper, we present the fabrication process of our silicon photonic platform to address optical communication application at 25 Gb/s and above, from Long-Haul networks to short reach data interconnects. This R&D platform on 200mm SOI wafers exhibits several advantages. Indeed, this platform is evolutionary allowing the addition of new modules or functionalities to extend the targeted applications. For instance, we can mention the heterogeneous integration of IIIV material to make lasers, electro absorption modulators, and optical amplifiers, the integration of edge coupler for large bandwidth applications, and the micro-bumping back end of line for 3D staking of electronics on photonics. The mature devices on this platform are implemented in a Physical Design Kit. Moreover, this platform is compatible with DAPHNE, the R&D platform on 300mm SOI wafers developed at ST-Microelectronics (Baudot, 2016). Finally, we present a strategy to address very high integration level for optical network on chip architectures. This strategy is based on implementing multi-layer photonic circuits on the same die. The benefit of such an approach is detailed at a component level for a ring resonator.

2 FABRICATION PROCESS

Wafers are fabricated in a fully CMOS compatible 8 inches fab at CEA-LETI. Starting materials are Silicon-On-Insulator (SOI) substrates featuring a 310nm thick silicon film on top of an 800nm thick

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Buried Oxide (BOX); handling wafers use high resistivity silicon. A modular approach is used to build the process flow that supports various sets of devices. The simplest process flow allows to fabricate passive devices only meanwhile, the full process includes the fabrication of active devices such as photodiodes and modulators as well as tuning capability using a thermal heater option. Figure 1 shows the overall technology integration scheme.

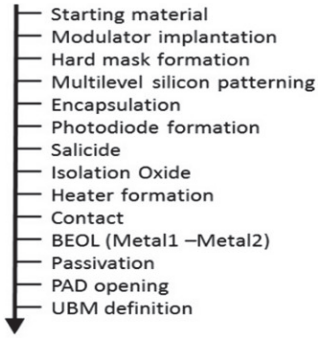

Figure 1: CEA-LETI photonic process integration scheme. A modular approach is used, meaning that the process can be adjusted with respect to the required devices.

The main devices needed to fabricate a conventional photonic chip are shown in the schematic cross-section of Figure 2. Tilted Scanning Electron Microscopy (SEM) pictures show some of the device fabricated. The front end modules will be described in the next sections. The proposed Back End Of the Line (BEOL) consists in 2 Al-Cu interconnection levels with W plugs and vias. A thick metal layer is used in order to improve RF performances thanks to low access resistances. An optional metal heater can be added within the oxide layer between the silicon and the first metal layer. A thin TiTiN layer is used to that end. Dedicated vias are then used to connect the heater level to the first metal contact layer. An additional Under Bump Metallization (UBM) process is available. The last feature is used for packaging, in particular for electronic Integrated circuit (IC) assembly on top of Photonic IC (Boeuf, 2015).

3 EDA SUPPORT

One key advantage of silicon photonics is that is uses the production capacities of CMOS foundries (e.g. big volume and low cost manufacturability). Another important aspect for the platform spreading is the use of a design flow based on the existing CMOS one. For

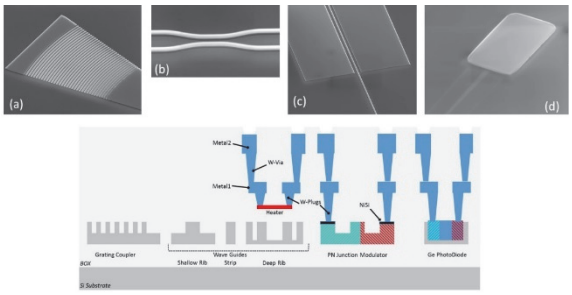

Figure 2: Schematic cross section of a photonic chip. Multiple level silicon patterning is used to define passive and active devices. The planarized BEOL is based on conventional 0.18µm CMOS interconnection levels. Top pictures are tilted SEM images of (a) 1D grating coupler, (b) shallow rib wave guides, (c) a Mach-Zendher Interferometer (MZI) modulator arm and (d) a Ge photodiode at the end of a waveguide.

a designer, a Physical Design Kit (PDK) is the gateway to the technology; it is then also strategic for silicon photonic foundries to propose PDK compatible with widely diffused EDA tools. Figure 23 presents the design flow developed in the frame of PLAT4M project to support CEA-LETI silicon photonic platform. It is close to what is done for CMOS process, except the Optical Rule Check module which has been specifically developed in order to validate the signal path integrity, checking if connection path exists between an input coupler and an output coupler. This feature can be seen as the ERC (Electrical Rule Check) proposed within the CMOS support EDA tools.

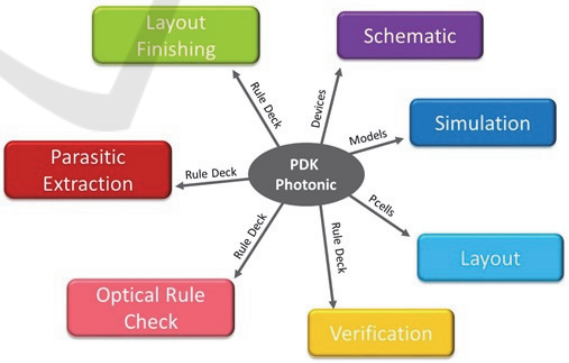

Figure 3: Supported silicon photonics design flow.

This part of the PDK includes the Schematic, Simulation and Layout boxes of the previous diagram. For all the supported devices, a model and a layout view are proposed. The optical bus used to simulate the devices has been extensively presented (Martin, 2014). It consists in a 9 lines structures. This bus can deal with light polarized along two axes and

account for light reflection which is not the case if only power and phase are used to represent the optical signal as it is often done. Native device models are developed in the Verilog-A behavioral language which has the main advantage of being supported by most of the SPICE commercial simulators.

Layout view proposed in the PDK are either fixed cells (for grating coupler for instance) or parametric cells. In that case some specific features related to the photonic specificities have been added. For instance, since photonic designs are not following the CMOS Manhattan configurations, it is useful to have some information like to overall optical length or the minimum radius for bended structures. It is done using callback in the user environment when instantiating a cells as illustrated in Figure 24 in the case of an S-Bend wave guide.

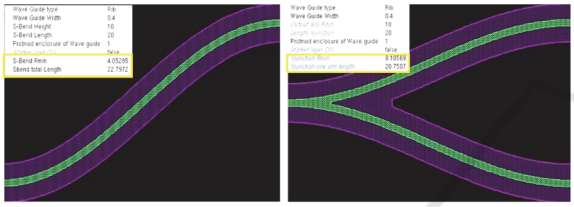

Figure 4: Layout views for S-Bend (left) and Y-junction (right). Insets are the user parameters in which are highlighted the additional information on radius and optical path length calculated from instantiation parameters.

Table 1 is an extract from our PDK device library with indicative performance for applications at 1310nm. All the devices fully supported by the platform's PDK. Specifications are given for designer's information; they are, most of the time, associated with the worst case corner of the device models. Complete behaviours of the devices are described in their Verilog-A models.

Design Rule Checking (DRC) is used to ensure that the geometric layout of designer contribution is compliant with rules which are described in the Design Rule Manual (DRM) to have a reliable fabrication and acceptable functional yield. However, trouble emerges when performing DRC on the photonic layout which is full of non-Manhattan geometries (spikes, tapers, etc.) and curvilinear shapes. This is expands the complexity of the DRC tasks. New and dedicated rules must then be developed. To do this, two main developments were made: introduction of new capabilities for layout verification tools (Cibrario, 2014) and creation of a design rules library (DRL) specific to silicon photonics.

Table 1: Extract from the PDK device library for 1310 nm operation.

Device	Specification	Value
Straight rib waveguide	Loss	<2.5 dB/cm (W=400nm) 0.25 dB/cm (W=1.8µm)
Straight strip waveguide	Loss	<4 dB/cm
Bend (R=5µm) strip waveguide	Loss	0.015 dB/90°
Fiber grating coupler	Insertion loss 1dB bandwidth	< 3 dB 30nm
Germanium photodiode	OE bandwidth @ -1V Responsivity Dark current @ 20°C	> 30 GHz 0.75 A/W < 10 nA
MZI modulator	EO bandwidth @ -2V Length Insertion loss Vpi @ -2V	> 20 GHz 4 mm < 8 dB 5 V
Ring modulator	EO bandwidth @ -2V DC Insertion loss Vpp RF @ -2V DC ER RF ER	15 GHz < 0.5 dB 0.8V 18dB 3.5dB
Ring filter	Quality factor Free Spectral Range Thermal tuning loss Extinction Rate	12000 6.6nm 0.4nm/mW <0.5dB 18 dB
MUX 100GLR4 WDM	Channel separation Bandwidth @ -1 dB IL over bandwidth Crosstalk over bandwidth	4.53nm 2nm 4dB > 18 dB
MUX CWDM	Channel separation Bandwidth @ -1 dB IL over bandwidth Crosstalk over bandwidth	20nm 13nm 4dB > 15 dB

To adapt the complex geometrical design of photonic integrated circuits (PIC), we use new capabilities for DRC, i.e. equation-based DRC, which are mostly used in advanced CMOS technology. This extends the capability of traditional DRC and allow users to analyze complex, multidimensional interactions (Figure 5) and addressed in this manner a new way to write rules check (Cao, 2014). To tackle grid snapping effect (Figure 6) which create lots of false errors, a tolerance value is introduced for some rules.

Using a new approach to write design rules with a high-level description language offers noticeable modularity and reusability through a generic Design Rule Library (DRL) concept. This methodology fastens and simplifies DRC rules file writing by allowing substantial reduction of the number of lines

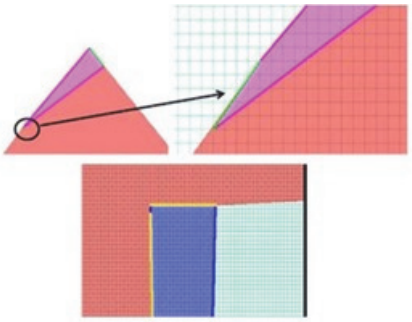

Figure 5: Errors not filtered by traditional DRC (without equation-based DRC).

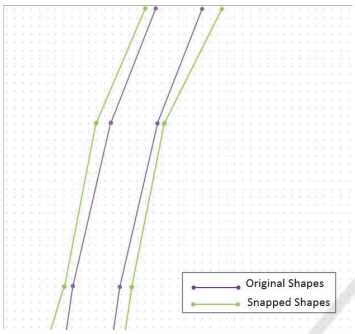

Figure 6: Width modification introduced by the snapping effect.

while keeping the possibility of using the latest DRC capabilities. This concept improves the robustness of the physical verification, thus reducing the risk of errors.

4 TECHNOLOGY PLATFORM EVOLUTION

As our platform aims to address various applications and needs, some new functionalities are continuously added. Typically, we develop the heterogeneous integration of IIIV material (Duprez, 2016) for lasers (Figure 7), electro absorption modulators, and optical amplifiers, the integration of edge couplers for large bandwidth applications, and micro-bumping back end of line for 3D staking of electronics on photonics.

These developments mainly address the optical communication transceiver roadmap. On one hand, we consider the data rate increasing towards terabit speeds which require high speed modulators and photodetectors, wavelength multiplexing, and advanced modulation formats. On the other hand, we

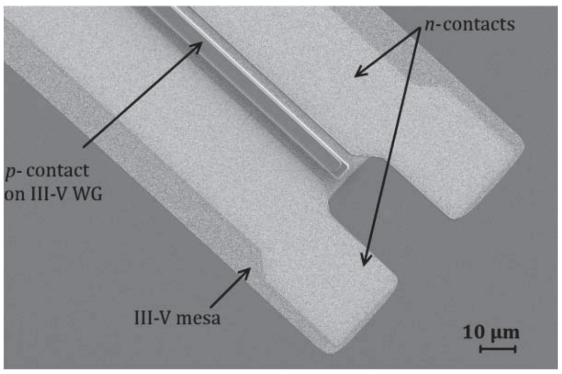

Figure 7: Heterogeneous integration on silicon of IIIV laser source.

consider the requirement to move photonics from front panel modules to mid-board modules in order to place it closer to high performance electronics.

The next integration step of photonics with electronics appears to be the development of optical network on chip (NoC) for high-performance computing (Thonnart, 2014). Indeed, comparing with electrical interconnects, photonics unique features such as: low latency leading to no fundamental difference between on-chip and off-chip links, high speed end-to-end network paths, high bandwidth density NoC, low power consumption, and high integration level. Moreover, photonics enable the evolution towards new architectures and resource management such as: architecture with unified switched photonic network, single writer – multiple reader optical buses, high-speed low-latency optical memory for reduced cache levels and optimized memory coherence, partitioning strategies for wavelength-routed optical NoC, or wavelength reservation protocol for reconfigurable optical NoC.

In order to anticipate this evolution of the requirement from gigabits per module to terabits per square centimeter, we prepare our photonic platform to be compatible with the integration of multi-layer silicon photonic circuits. Indeed, this integration should be mandatory to deal with highly integrated circuits such as routers or optical network on chip described previously. In this approach, for instance, at least two silicon photonic circuits will operate together. The silicon waveguide layers are close enough (i.e. 100nm) to deal with efficient optical coupling. Regarding the packaging, these circuits will share the same BEOL (Figure 8).

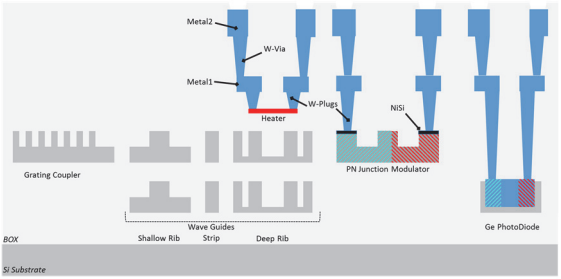

Figure 8: Schematic cross section of a photonic chip with 2 photonic circuit layers.

This integration scheme offers a new degree of freedom to designers both to improve the performance of the existing components, and to develop new functions. The development of this multi-layer photonic platform is programmed in two steps: first with passive components, second with active components.

As a first example, we present the design of a ring resonator with the ring waveguide being processed on the upper circuit. In this design the upper circuit is patterned on a 304nm thick amorphous silicon layer with 100nm of intervening SiO2 (Figure 9).

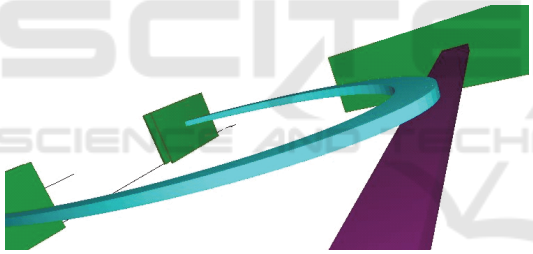

Figure 9: Ring to waveguide coupling structure for FDTD simulation.

The coupling coefficients between a straight strip-type waveguide and a curved waveguide with a constant 5µm radius have been simulated using 3D-FDTD. Figure 10 shows that for a given SiO2 thickness and waveguide offset, the coupling coefficient is relatively stable for typical variations of waveguide geometry. For example, with identical waveguides of 304/350nm height/width a SiO2 thickness of 100nm and a waveguide offset of 300nm gives a coupling coefficient of -15.1dB (3.1%), ±10nm variations in the height and width of the input/output waveguides lead to at worst -15.1±1dB (2.5-4%) variations in the coupling coefficient.

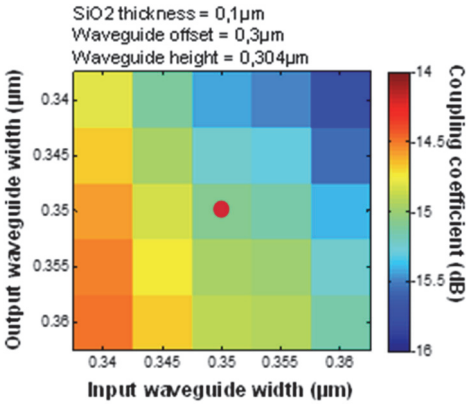

Figure 10: FDTD simulation results of the coupling coefficient between a straight waveguide and a superposed curved waveguide.

This coupling structure shows benefit both for passive and active functions. Indeed, as a passive function it will be used as a wavelength selective coupler between the upper circuit and the lower circuit. It is a relevant degree of freedom for switching circuits which require thousands of crossings (Testa, 2016). As an active function, it enables the modulation of the entire ring circumference which will significantly improve the performance for small ring radii (i.e. less than 5µm).

5 CONCLUSION

Silicon photonics exhibits now a high level of maturity to develop next-generation high speed transceivers for optical fibre networks. This maturity is based on the research effort from academia and industry by using conventional silicon integrated circuit infrastructure with Electronic Design Automation tools, CMOS foundries, and wafer-level testing. The CEA-Leti 200mm R&D platform has fueled the demonstration of multiple applications (Bernabé, 2016). Now, the evolution of this platform is mainly based on heterogeneous integration of IIIV material to make laser source, and multi-layer photonics to address the high density level of optical network on chip.

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