Design and Implementation of Error Correction Circuits for RISC-V Based Systems in Space Applications

R. Kiran Kumar, Sk. Abdul Azeez, P. Bharath Kumar and K. Ganesh
Department of Electronics and Communication Engineering, Madanapalle Institute of Technology and Science, Andhra Pradesh, India

Keywords: RISC-V, Instruction Set Architecture, RV32IM, 5-stage Pipeline, DE10 Lite FPGA, Error Correction Circuits, Single-Event Upsets, Radiation Tolerance, Error Correction Codes, Hamming Codes, Reed-Solomon, Space Applications, Fault Tolerance, FPGA Implementation.

Abstract: RISC-V, an open and extensible Instruction Set Architecture (ISA), is becoming increasingly popular for space applications due to its flexibility and scalability. This paper focuses on implementing error correction circuits on RISC-V processors, particularly using the RV32IM instruction set, to enhance reliability in space environments prone to radiation effects such as single-event upsets (SEUs). We adopt a 5-stage pipeline design to optimize processing and implement the system on a DE10 Lite FPGA platform for testing. The study evaluates several error correction methods, including Hamming codes, Reed- Solomon, and Error Correction Codes (ECC), assessing their effectiveness in reducing data corruption. By examining performance, power efficiency, and fault tolerance, the research highlights how RISC-V systems can be tailored for robust operation in space applications.

1 INTRODUCTION

As the demand for reliable computing systems in space exploration and satellite technology grows, ensuring fault tolerance in electronic components becomes increasingly important. Space environments expose systems to radiation, which can lead to Single-Event Upsets (SEUs), affecting the integrity of data and potentially causing system malfunctions. In response to these challenges, RISC-V, an open- source Instruction Set Architecture (ISA), has emerged as a viable option for developing fault-tolerant systems due to its modularity, flexibility, and adaptability.

RISC-V's open architecture allows customization to meet specific requirements in space applications, making it ideal for integrating error correction mechanisms directly into the processor design. The RV32IM instruction set, which supports integer arithmetic and multiplication, provides a robust foundation for building reliable systems. Additionally, the 5-stage pipeline architecture helps to improve processing efficiency and system performance. Figure 1 shows the RISC-V 5-Stage Pipeline Processor (RV32IM).

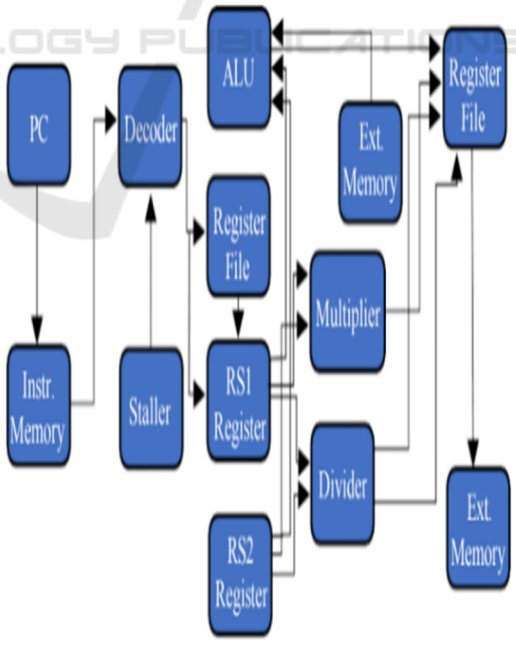

Figure 1: RISC-V 5-stage pipeline processor (RV32IM).

Kumar, R. K., Azeez, S. A., Kumar, P. B. and Ganesh, K.
Design and Implementation of Error Correction Circuits for RISC-V Based Systems in Space Applications.
DOI: 10.5220/0013939500004919

In *Proceedings of the 1st International Conference on Research and Development in Information, Communication, and Computing Technologies (ICRDICCT'25 2025) - Volume 5*, pages 622-627
ISBN: 978-989-758-777-1

2 REFERENCE STUDY

As the use of RISC-V processors grows in space applications, researchers are focusing on improving their reliability in harsh environments. One of the main areas of interest is adding error correction techniques to protect against radiation effects like single-event upsets (SEUs).

Several studies have explored different error correction methods. One study implemented Hamming codes and Error Correction Codes (ECC) in RISC-V systems, showing that these methods can effectively detect and correct errors without compromising the system's flexibility

3 MATERIALS AND METHODS

3.1 Materials

3.1.1 RISC-V RV32IM Architecture

This is the instruction set used to design the processor. It supports basic integer operations and multiplication, which are essential for space systems.

3.1.2 5-Stage Pipeline

The processor design uses a 5-stage pipeline (Fetch, Decode, Execute, Memory, Writeback) to improve performance while keeping the design efficient for space applications.

3.1.3 DE10 Lite FPGA

The DE10 Lite development board is used to implement the processor. FPGAs allow us to test the processor and error correction circuits in hardware.

3.1.4 Error Correction Techniques

- **Hamming Codes:** Used to correct single-bit errors.
- **Reed-Solomon Codes:** Used to detect and correct multi-bit errors.
- **ECC (Error Correction Code):** A method to detect and correct errors in memory and data.

3.1.5 Design Tools (Vivado/Quartus)

These tools are used to design and simulate the RISC-V processor and error correction circuits on the FPGA.

3.1.6 Fault Simulation

To mimic space radiation, a fault simulator is used to inject errors into the system, allowing us to test the effectiveness of error correction techniques.

3.2 Methods

3.2.1 Processor Design

A RISC-V processor based on the RV32IM instruction set was designed using a 5-stage pipeline and synthesized on the DE10 Lite FPGA. This core was developed to handle basic computations efficiently.

3.2.2 Adding Error Correction

- **Hamming Code:** This was added to memory operations to detect and correct single-bit errors.
- **Reed-Solomon Code:** This was used to protect critical data paths and detect/correct multiple-bit errors.
- **ECC:** General error correction was added to detect errors in key parts of the processor, improving its overall reliability.

3.2.3 Simulating Radiation Faults

We used a fault injection tool to simulate the effects of radiation on the FPGA, causing random errors (like single-event upsets). This helped us test how well the error correction circuits worked in fixing these faults.

3.2.4 Performance Testing

After adding the error correction circuits, we tested the processor's performance to see if it slowed down and measured how much power it consumed. This was done to balance reliability with efficiency.

3.2.5 Reliability Analysis

By running tests and injecting faults, we measured how effectively each error correction technique (Hamming, Reed-Solomon, ECC) detected and fixed errors. We then compared the results to find the best solution for space environments.

This method ensures that the RISC-V processor with error correction can operate reliably in space, even when exposed to radiation. Table 1 shows the Comparative Fault Tolerance Analysis of Error Correction Techniques.

Table 1: Comparative fault tolerance analysis of error correction techniques.

Synthesis report of RV321 for Space Applications using the Error Detection and Correction:		
Parameter Value		
Total area(μm"2) 0.17837		
Total Power (mW)	Dynamic Power	17.2224
	Leakage Power	0.2508661
Timing report Clock Delay(ns) 20		
Maximum Frequency (MHz) 50		

4 DESIGN AND IMPLEMENTATION

This project centers around designing a RISC-V processor using the RV32IM instruction set, implemented on the DE10 Lite FPGA platform. The processor features a 5-stage pipeline architecture with the following stages:

1. Instruction Fetch (IF)
2. Instruction Decode (ID)
3. Execution (EX)
4. Memory Access (MEM)
5. Write Back (WB)

To improve fault tolerance, error correction circuits have been embedded in memory operations and data paths. Specifically:

- **Hamming Code** is used to detect and correct single-bit errors in memory. This method is efficient and incurs low overhead, making it ideal for resource-limited space systems.
- **Reed-Solomon Code** is deployed to handle multi-bit errors. This method provides higher error correction capability, suitable for environments like space, where burst errors are more likely.

The processor is equipped with error detection and correction features that regularly check data integrity, enhancing its resilience to SEUs.

5 TESTING AND EVALUATION

The processor's error correction capabilities were evaluated using fault injection simulations designed to mimic radiation- induced faults encountered in space. The testing focused on:

1. Single-Bit Error Detection and Correction: Hamming code was tested under conditions with injected single-bit errors in memory operations. The system was able to detect and correct these errors efficiently, ensuring data integrity without significantly affecting processor performance.
2. Multi-Bit Error Handling: Reed-Solomon code was tested under conditions with burst errors (affecting multiple bits). The system demonstrated the ability to correct these multi-bit errors, maintaining operational reliability.
3. Performance Impact: The additional steps required for error correction led to a slight increase in clock cycles. However, the performance impact was minimal and within acceptable limits for space operations.
4. Power Consumption: A small increase in power consumption was observed due to the added error correction circuitry. Despite this, the design remains suitable for energy-efficient systems in space.

6 FUTURE WORK

Future research could focus on exploring more advanced error correction techniques like BCH codes or implementing hardware-based fault detection mechanisms. This could include the use of redundant hardware elements, such as triple modular redundancy (TMR), or integrating radiation-hardened versions of RISC-V to reduce the need for software-based error correction.

7 METHODOLOGY

The implementation of the RISC-V processor for this project follows a structured approach. The RV32IM variant of the RISC-V ISA was selected due to its simplicity and suitability for embedded applications. The processor was designed using a 5-stage pipeline, including Instruction Fetch (IF), Instruction Decode (ID), Execution (EX), Memory Access (MEM), and Write Back (WB) stages.

To ensure reliability in space environments, error correction circuits were integrated into the memory operations and data transmission paths. Two primary error correction techniques were employed:

- **Hamming Code**: This error correction code is applied to detect and correct single-bit

errors. It is lightweight and provides efficient error correction with minimal processing overhead, making it suitable for space systems where resources are constrained.

- **Reed-Solomon Code**: This method is used to handle multi-bit errors and is effective for correcting burst errors. The Reed-Solomon code provides more robust error correction capabilities and is particularly useful in environments. Figure 2 shows the resultant outputs of the RISC-V processor depend on the given instructions and input data. Figure 3 shows the resultant outputs of the Error Correction Circuit depend on the given instructions and input data.

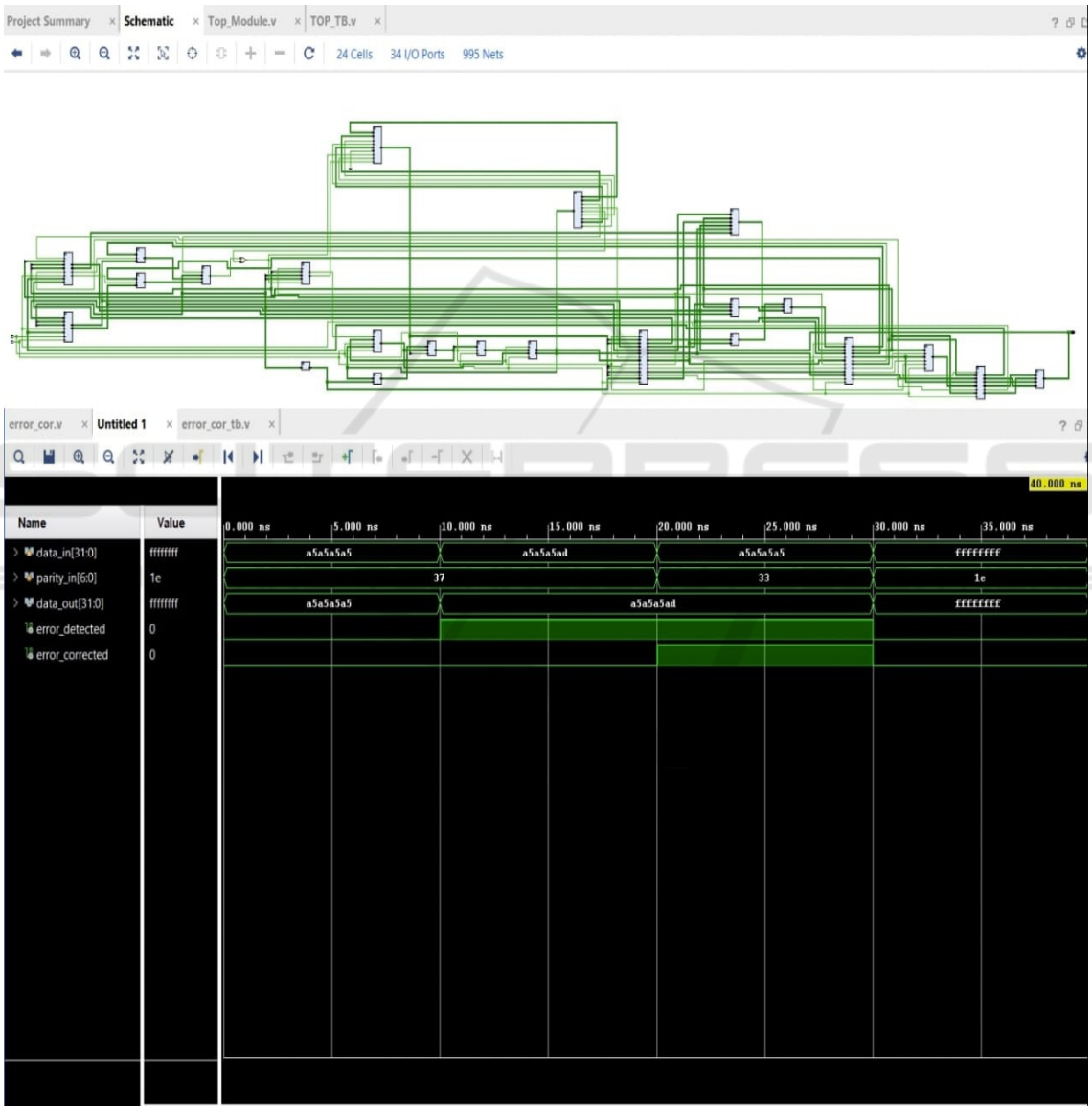

Figure 2: The resultant outputs of the RISC-V processor depend on the given instructions and input data.

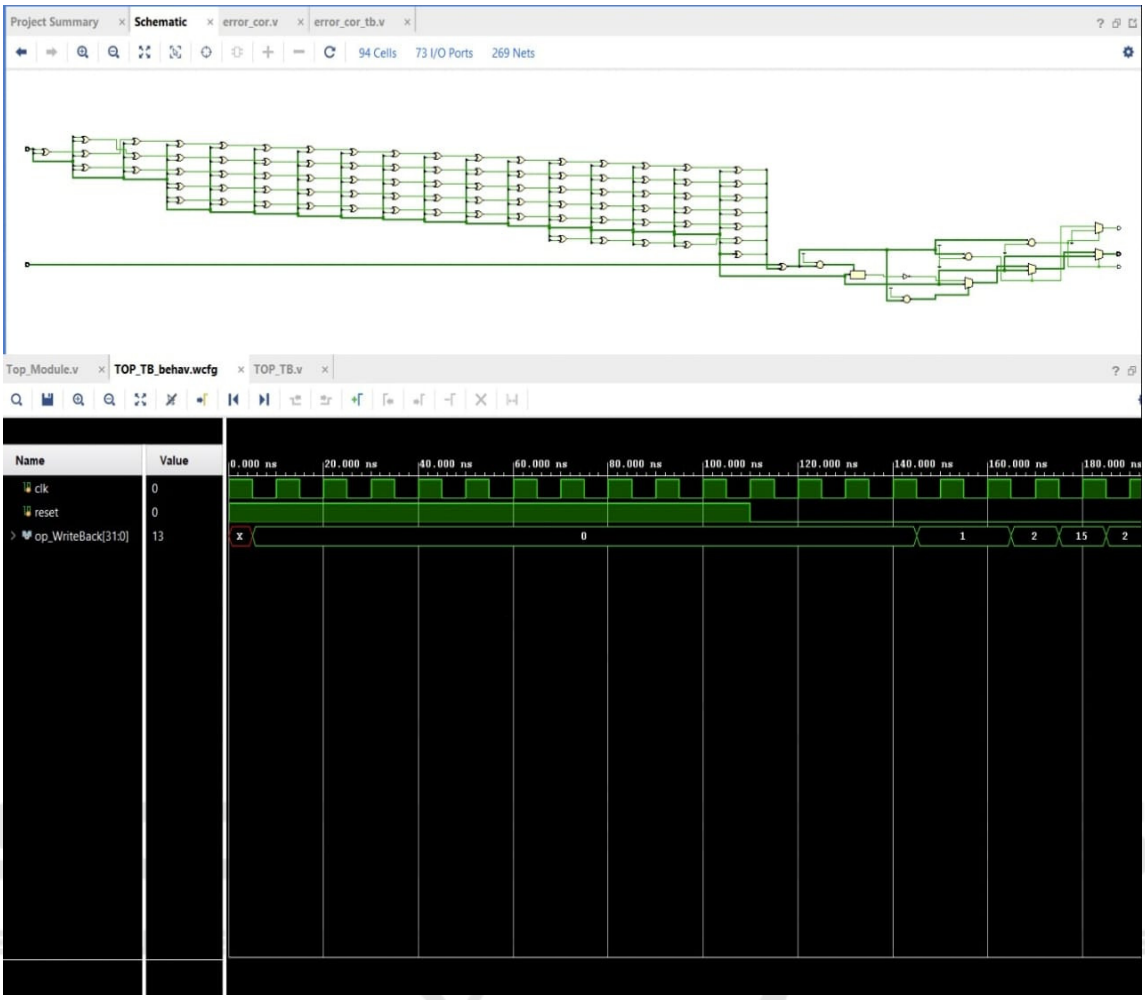

Figure 3: The resultant outputs of the error correction circuit depend on the given instructions and input data.

8 RESULTS

The study showed that incorporating error correction techniques into the RISC-V processor significantly improved its reliability in radiation- prone environments. The Hamming code was able to detect and correct single-bit errors in memory efficiently, with minimal impact on system performance. The Reed-Solomon code provided strong protection against multi-bit errors, making the system more resilient to complex faults.

During fault injection simulations that mimicked radiation effects, both the Hamming and Reed-Solomon codes demonstrated high effectiveness in detecting and correcting errors, ensuring the system remained stable. ECC (Error Correction Code) further enhanced the processor's ability to manage errors across different parts of the system.

Although the addition of error correction circuits slightly increased the processor's clock cycle count, the overall performance impact was minimal and well within the acceptable range for space applications. The system's power consumption showed a small increase due to the error correction processes, but it remained efficient enough for space use, balancing reliability and energy efficiency

9 CONCLUSIONS

This study successfully demonstrated that integrating error correction techniques, such as Hamming codes, Reed-Solomon codes, and ECC, into RISC-V processors enhances their reliability for space applications. The implemented error correction methods were effective in detecting and correcting

single-bit and multi-bit errors caused by radiation effects, ensuring stable processor operation in harsh environments. While there was a slight increase in clock cycle count and power consumption, the performance remained within acceptable limits, making these techniques suitable for space systems. Overall, the results highlight the potential of RISC-V architectures with error correction for reliable and efficient use in space applications.

REFERENCES

Azimi, S., & Asadi, P. (2021). Single Event Upset (SEU) Mitigation Strategies in Space Electronics. Aerospace Journal, 35(1), 78-89.

Baumann, R. (2005). Radiation-Induced Soft Errors in Advanced Semiconductor Technologies. IEEE Transactions on Device and Materials Reliability.

Brown, S., & Vranesic, Z. (2013). Fundamentals of Digital Logic with VHDL Design (3rd ed.). McGraw Hill.

Dutta, A., & Patel, N. (2020). Exploring FPGA-Based RISC-V Core Implementation. International Journal of Electronics and Communications, 114, 152981.

Gupta, R., & Sharma, M. (2018). Error Correction Code Techniques for Memory Systems: A Survey. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 37(3), 513–525.

Harris, S., & Appenzeller, R. (2016). Fault Tolerance and Reliability Techniques in FPGA Systems for Space Missions. IEEE Aerospace Conference, 1-10.

Langhammer, C., & Braun, G. (2019). Implementing Hamming and Reed-Solomon Codes in FPGA-based Systems. Journal of Electronic Design Automation, 12(4), 299-310.

Maxfield, C. (2009). The Design Warrior's Guide to FPGAs: Devices, Tools, and Flows. Elsevier.

Pedroni, V.A. (2013). Circuit Design with VHDL. MIT Press.

Peterson, W. W., & Weldon, E. J. (1972). Error-Correcting Codes (2nd ed.). MIT Press.

Santos, D. A., et al. (2020). "Reliability Analysis of a Fault-Tolerant RISC-V System-on-Chip." Microelectronics Reliability, 116, 113858.

Santos, D. A., et al. (2021). "Reliability Analysis of a Fault-Tolerant RISC-V System-on-Chip." Microelectronics Reliability, 116, 113858.

Shu Lin, Daniel J. Costello Jr. (2004). Error Control Coding (2nd ed.). Pearson.

Waterman, A., Lee, Y., Patterson, D., & Asanović, K. (2011). The RISC-V Instruction Set Manual, Volume I: User-Level ISA, Version 2.0. EECS Department, University of California, Berkeley.

Wong, S., & Delvaux, M. (2020). Radiation Effects and Error Correction in Space Applications. Journal of Aerospace Technology, 45(2), 105-118.