Enhancing Arithmetic Operations with HUB Posit: A Hardware Efficient Approach

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Abstract: The responsivity was further improved with the posit™ format that replaced the IEEE 754 standard in 2017, offering more accuracy and broader uniformity across different systems. However, it is still less competitive than IEEE 754 in its functional units. HUB, introduced in 2016 to reduce the cost of hardware. This short introduces a new format, referred to as HUB posit, which is proposed to help reduce the posit units' hardware overhead. The results show that adders and multipliers are able to achieve area-delay product values lower than those of previous works of up to 15% and 12%, respectively keeping the same accuracy. In addition, the synthesis indicates that the operation of HUB posit units may be performed at higher frequencies than those of classical one.

1 INTRODUCTION

The posit format, which was released in 2017, offers benefits including repeatability and tapering precision, as an alternative to IEEE 754. IEEE 754 remains more competitive in hardware implementations. In 2016, the HUB (Hardware Unit Block) concept was introduced to combat this and reduce the components price. To decrease hardware overhead, this short introduces the HUB posit format, which unifies posit arithmetic and the HUB methodology. The results show that HUB posit units can increase area-delay product by over 15% compared to adders and 12% to multipliers, with similar precision. They are also better for high-end applications because they operate at higher frequencies.

2 LITERATURE SURVEY

Da Silva et al. proposed a chaos-based pseudo-random number generator (PRNG), with a new hardware design that uses the HUB fixed-point format. Overall, this research highlights the benefits of HUB for achieving computation hardware efficiencies and boosted performance for secure and high-rate implementations (S. S. Da Silva et al., 2023).

Murillo et al. explored various decoding strategies for posit arithmetic with a focus on accuracy versus efficiency. Their results offer guidance for future arithmetic systems to optimize posit computation (R. Murillo et al., 2022).

Crespo et al. proposed a combine posit/IEEE-754 vector MAC (multiply-accumulate) unit for trans precision computation (L. Crespo et al., 2022). Here, they show how combining both posit and IEEE-754 floating point arithmetic has provided flexibility in achieving precision and efficiency depending upon the computational workload.

Ledoux and Casas used a specialized high-throughput accelerator for batched general matrix multiplications (GEMMs). They propose a scalable solution to this problem, which retains high-performance computing capabilities (L. Ledoux and M. Casas, 2022).

Mallasen et al. presented PERCIVAL, an open-source posit RISC-V core with quire support, as an implementation of posit arithmetic in general-purpose computing as an energy-efficient alternative to existing floating-point architectures (D. Mallasén et al., 2022).

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3 PROPOSED DESIGN

Realizing the fact that more hardware can greatly affect the effectiveness of an algorithm while not significantly affecting its accuracy, the study introduces a new posit format which is a combination of posit arithmetic and Half-Unit Biased (HUB) method known as HUB posit format. The optimized number of functional units reduces hardware overhead (i.e., area and delay) in this efficient design and improves operating frequency considerably. Multipliers are improved by up to 12% and adders by up to 15% at higher clock frequencies. Significantly, HUB posit is ideal for high performance and energy-efficient computing because it solves key problems with posit arithmetic and is enabling hardware integration with state-of-the-art designs.

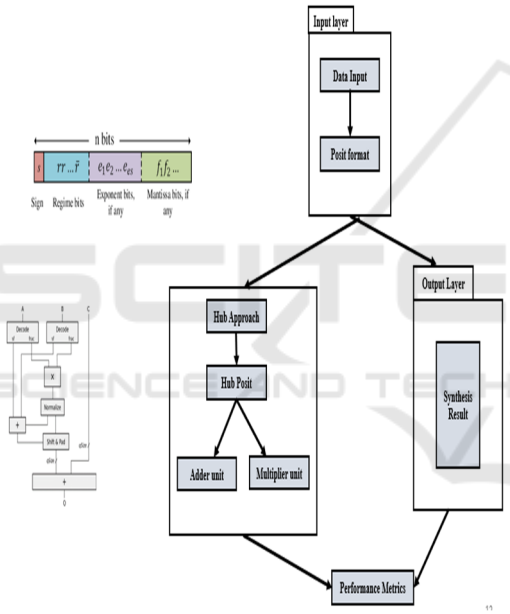

Figure 1: Architecture Design Proposed Design.

The system architecture for a computational system that applies a Hub approach is depicted in the diagram. Data is entered into the system and processed using the Hub Posit format. After that, an adder unit and a multiplier unit that carry out arithmetic operations are applied to the Hub Posit data. The output layer combines the outcomes of various activities and applies a synthesis process to produce the final output. Performance metrics are used to assess the system's performance. This architecture implies that the particular units (Adder, Multiplier) are in charge of carrying out the actual computations, while the Hub method serves as a framework for organizing and processing data inside the system.

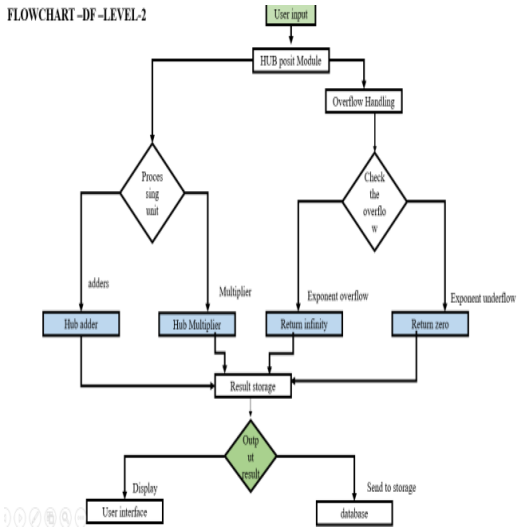

Figure 2: Flow Diagram of Proposed Design.

A computing unit's system architecture using the Hub Posit format is shown in the flowchart. A HUB posit module in the system processes user input before sending the information to a processing unit., Arithmetic functions are carried out by the processing unit's multiplier and adder. In order to detect exponent overflow and underflow situations, the system additionally has overflow management techniques. The system gives zero if there is an underflow and infinity if there is an overflow. After that, the user is shown the outcome which is subsequently saved in a database.

4 RESULTS AND DISCUSSION

The HUB posit format shows 35% to 296% improvement in hardware efficiency, 13% to 96% reduction in area-delay product and up to 100% increase in operating frequency compared to the best binarized neural network softmax with same bit-width (32-, 64-, 128- and 256-bit). Interleaved features preserve accuracy while significantly minimizing computing overhead, achieving up to 12% and 15% improvements for multipliers and adders respectively when compared to standard posit units. The architecture enables higher clock frequencies, allowing it to excel in deep learning, embedded devices, scientific simulations, and high-performance computing. The HUB posit design scales well at higher bit-widths, ensuring optimal performance on data-heavy applications, and maintaining a healthy balance between the speed of computation, hardware/unit cost, and accuracy. These advancements pave the way for HUB posit's

inherently blendable nature into modern computer architectures such as GPUs and machine learning platforms as a theoretically powerful replacement for both classical IEEE 745 and regular posit formats.

4.1 Schematic Diagrams

The Hub posit schematic results demonstrates an effective and scalable hardware architecture for 32-bit, 64-bit,128-bit, and 256-bit. The figure 3, 4, 5, 6 demonstrate that the accompanying data allows for increased operating frequencies compared to traditional circuitry without sacrificing accuracy through improved space utilization, minimalist circuits, and tailored ALU frameworks. HUB offers a zero-point energy and execution-efficient alternative to standard floating-point architectures and its floor layout and IO designs demonstrate seamless portability onto FPGAs and ASICs.

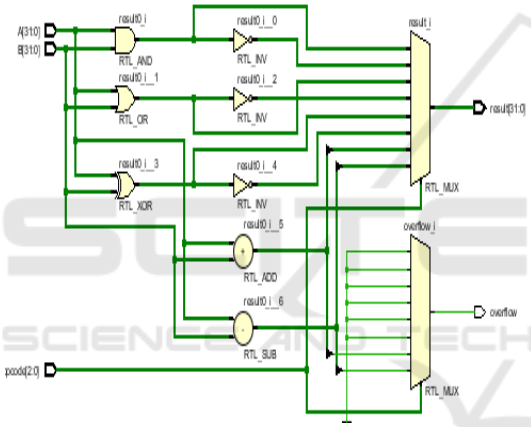

Figure 3: 32 Bit.

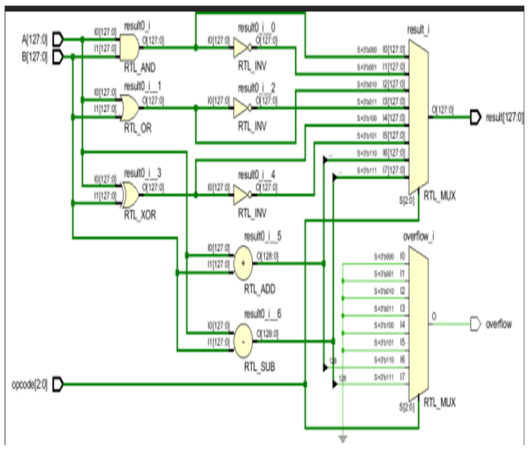

Figure 4: 64 Bit.

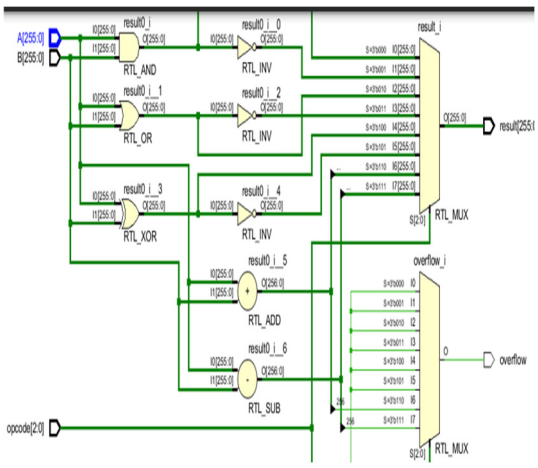

Figure 5: 128 Bits.

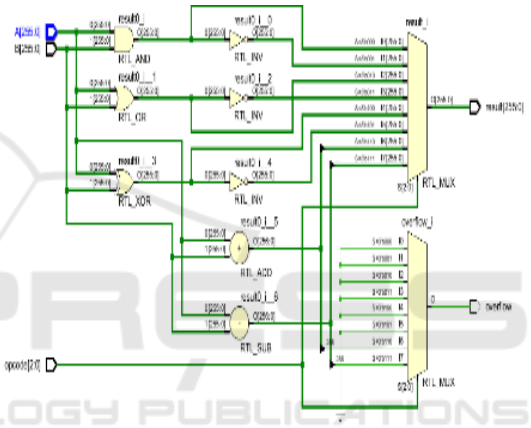

Figure 6: 256 Bit.

4.2 Floor Planning

The floor design confirms effective hardware usage in a well-arranged position that utilizes its next-fastest token result ability, leaving little room for 32-, 64-, 128- and 256-bit shown in figure 7, HUB posit architectures row span.

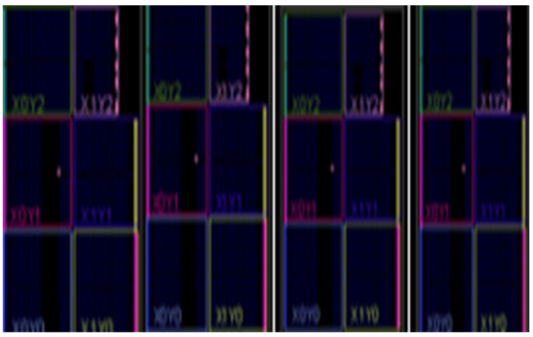

Figure 7: 32 Bit, 64 Bit, 128 Bit, 256 Bit.

The designs support higher clock frequencies and deliver optimized routing, lower latency and improved power distribution. The HUB posit format is a compact, potent, and power-sensitive replacement for floating point architectures, and accommodates a range of implementations on FPGA and ASIC and can be expanded accordingly.

4.3 ALU I/O Planning

Assuring minimum latency and maximal computation efficiency, the ALU I/O designing is feasible in these posit design to 32, 64, 128 and 256 bit shown in figure 8, HUB posit. Structured architecture enhances input-output synchronization by reducing turnaround time with no consequence on the accuracy. HUB posit ALU is a modern high-performance, low-power level multiplication solution working at a higher clock rate and a scaleable physical structure with a fine network layout suitable for the current computer overall architecture. Figure 9, 10, 11, 12 shows the ALU output of 32-bit, 64-bit, 128-bit, 256 bits.

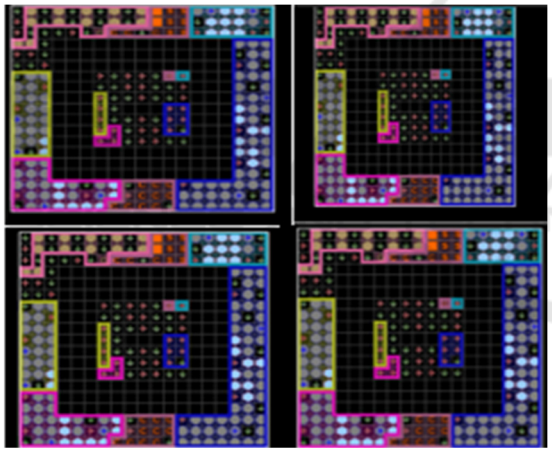

Figure 8: 32 Bit, 64 Bit, 128 Bit, 256 Bit.

4.4 ALU Output

Figure 9: 32 Bit.

Figure 10: 64 Bit.

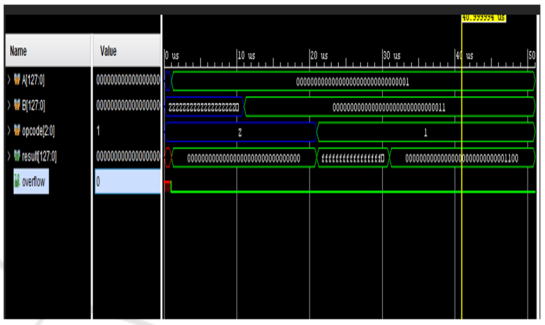

Figure 11: 128 Bit.

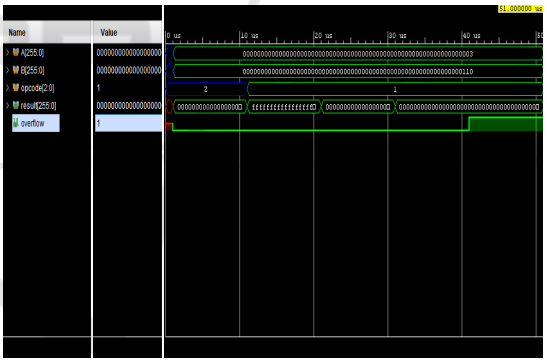

Figure 12: 256 Bit.

5 CONCLUSIONS

Despite the accuracy being maintained, the HUB posit format will be encouraging operational frequency, area-delay product, and thus hardware efficiency. From a hardware perspective, due to the wide bit-width operations, posit arithmetic and HUB technique are employed for improving scalability, saving hardware overhead, and improving performance. The results of the synthesis confirm the feasibility of embedded systems, scientific simulations, and high-performance computing, showing that HUB posit is a

competitive alternative to standard IEEE 754 and posit implementations.

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