A Scalable High-Speed Hybrid Full Adder Design Based on XOR-XNOR Gates

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Abstract: XOR-XNOR-based Full-swing Adder that is scalable and FinFET is described in this report. FinFET technology has been employed as an alternative to bulkCMOS in ultra-low power designs since it offers several advantages such as more effective channel management, reduced energy consumption, faster switching, and so on. Previous research has compared the influence of this new technology on the circuitand evaluated the performance gains that may be obtained. In comparison to the suggested adders, the state of the art comprises certain known adders in FinFET technology. The suggested full adders improve Silicon area by 19.35 percent, AveragePower by 33.59 percent, Propagation Delay by 36.15 percent, Area Delay Product (ADP) by 56.22 percent, and Power Delay Product by 57.59 percent as compared to theprevious full Adder. Compared to the Mirror CMOS full adder Furthermore, performance characteristics had been investigated. By increasing the in the extended adder structures, Full Adders to 32 bits are used without the addition of level restoringbuffers In-between stages. According to the modelling results, the planned full adder and 5 of the 11 current full adders can be increased to 32 bits in practice. The suggestedfull adder outperformed the competition. The 32-bit mode of operation the suggested hybrid full adder can be more effective due to its improved features and it can be a morestable and superior option than present full adders.

1 INTRODUCTION

Modern electronic gadgets must operate quickly and have a long battery life while having the lowest feasible footprint. Portability is also considered to be a major requirement in electronic devices. In battery-powered systems, the quantity of energy stored in the battery is fixed. As a result, energy dissipation is a critical aspect in battery-powered gadgets in order to extend the battery's average lifetime. Low-power circuits are predicted to use smaller batteries, be lighter, and last longer. Energy dissipation is also critical in deep sub- micron technologies. Developments in fabrication technology of CMOS get larger the number of transistors in every 2 years according to Moore’s laws, as a result the amount of electricity dissipated per unit area increases, causing the chip area of the circuit to expand. Excessive heat reduces the circuit designer's dependability and lifespan. In some cases, Low-power, high-performance circuits may be impossible to achieve. using complementary metal oxide semiconductor logic.

As a result, several other devices, such as FINFETs and CNTFETs, are being added to enhance speed, power consumption, and area. The FinFET transistor is one of the most significant in this field.

Introduction to VLSI: By combining several transistors generated on circuits into a single chip, VLSI is a method of creating integrated circuits. VLSI was born and during the development of sophisticated semiconductor and communication technologies in the 1970s. A VLSI device is the microprocessor. The microprocessor is a VLSI

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device. As chips have become more complicated, with hundreds of millions of transistors, the phrase is no longer as widely used as it once was. The industry in which ever-increasing numbers of logic devices are crammed into ever-tinier areas. Circuits that would have taken up a lot of space on a board may now be squeezed into a small space only a few millimeters wide thanks to VLSI. VLSI has been around for a great many years and is nothing new, however as a result of developments in computer technology, there has been a tremendous increase in the number of tools available to build VLSI circuits. In addition, following Moore's law, an IC's capabilities have grown dramatically over time in terms of compute power, space usage, and yield. People may now incorporate various functionality into ICs as a result of these two advancements, opening up new vistas. Placed systems, in which intelligent devices are embedded into common items, and ubiquitous computing, in which little computer devices spread to the point where even your shoes may do important tasks, are two examples.

Designers needed methods to combine numerous simulation levels, which is when Verilog was developed. In the early 1980s, there were functional simulators, switch-level simulators, and gate-level simulators (sometimes created on the fly in software), but no easy technique to connect them. In addition, traditional programming languages were/are primarily sequential, making them "semantically problematic" for simulating the concurrency of digital circuitry. Phil Moore of Gateway Design Automation invented Verilog in 1983-4, and a year later, the first simulator was developed.

2 LITERATURE SURVEY

Analysis of Hybrid Full Adders Using Logical Effort

The advantages of hybrid full adders are explored in this work, and hybrid full adders are also contrasted with traditional CMOS circuits. Compared to traditional CMOS circuits, Hybrid Full Adders Utilizing Logical Effort structures are faster and use less power. (Kumar, Gotam, et al. 2017), (Naseri, Timarchi, et al. , 2017), (Rajagopal, Chakrapani, et al. 2021), (Kandpal, Tomar, et al. 2020), (Hasan, Islam, et al. 2021)

XOR-XNOR module is used in a scalable high-speed hybrid 1-bit full adder architecture:

In this study, full adders based on XOR-XNOR are built, as well as compared with hybrid FA circuits based on XOR-XNOR, with outstanding results that allow these FAs to be used in digital arithmetic blocks of contemporary microprocessors.

Design of XOR-XNOR Topology Low Power High Speed Complete Adder Circuits: In this paper advantages of the full adders are discussed with the real time applications. (Wairya, 2012), (Jyothi, Rao, et al. 2020), (Subhashini, Kamaraj, et al. 2019), (Addagatla, Chelle, et al. 2022), (Prashanth, et al. 2022)

Introduction to FIN-FET:

A Fin field effect transistor is something of a transistor. It serves as both an amplifier and a switch because it is a transistor. Home PCs, laptops, tablets, smartphones, wearable technology, high-end networks, automobiles, and other gadgets are only a few of its applications. A fin-shaped field-effect transistor is referred to by the abbreviation "fin field effect transistor.". The name "fin" refers to the fin-shaped body of the transistor, which is distinguished by the silicon fin that serves as the main body. Field-effect because an electric field controls the conductivity of the substance. A Fin field effect transistor is a device that does not have a single plane.

It is sometimes referred to as 3D since it has a third dimension. (Prashanth, Sree, et al. 2023), (Raghunandan, Shilpa, et al. 2019), (Kadu, Sharma, et al. 2017), (Taherinejad, Abrishamifar, et al. 2009), (Balakumaran, Prabhu, et al. 2016), (Ramkumar, Gracin, et al. 2020)

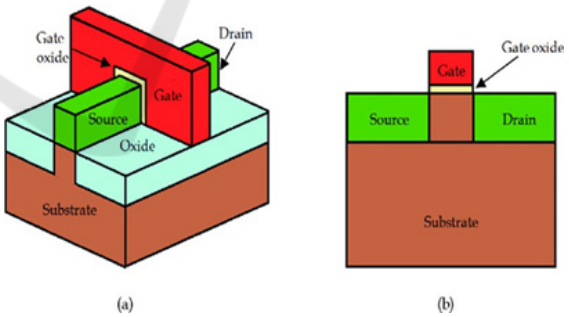

Figure.1: Structure of FINFET

3 CIRCUITS OF XOR, NOR AND FULL ADDER

The Basic binary circuits used for the designs are briefly explained here.

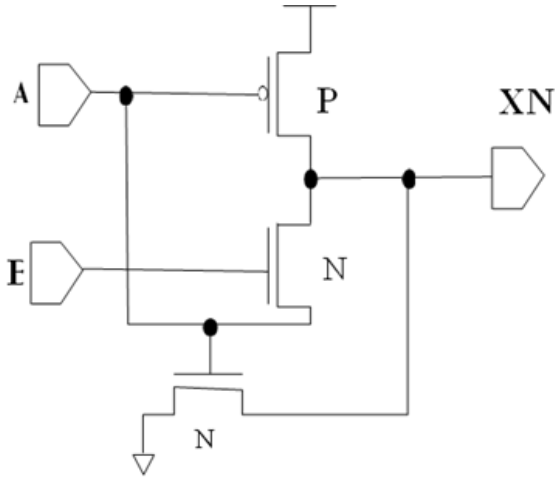

Figure 2: Circuits of XOR, NOR and Full Adder

The output of an XOR circuit is always 1 when the input is logic 1, and it is always 0 when the input is logic 01 or logic 10. Moreover, the output logic is always 0 when the input logic is 11.

3.1 XNOR circuit

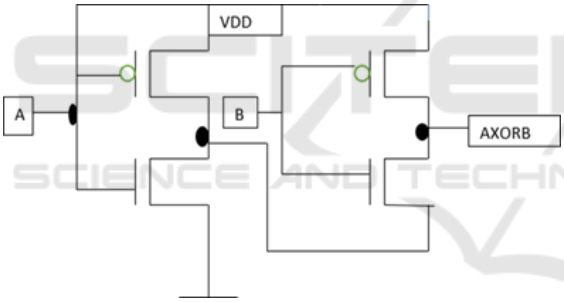

Figure-3: Schematic of XNOR

When the input is logic 0 0 for the XNOR circuit then, the output is logic is 1 and when the input is logic 01 or logic 10, then the output is logic is always 0. And when the input logic is 11 then the output logic is always 1.

3.2 Existing Models

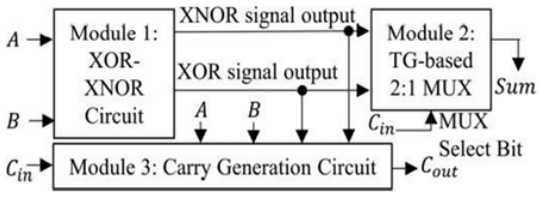

Figure 4: Schematic of Design-I

Here 3 blocks are combined together to form hybrid full adder circuit i.e., module-1 XOR-XNOR circuit, module-2 TG based 2:1 mux, module-3 carry generation circuit. And also, the output bits are A, B, Cin, and sum. It is composed of an XOR-XNOR module and a TG-based module that together provide the sum result and a separate carry generating module that accepts input from the XOR-XNOR module to give Cout output.

Table. 1. Existing CMOS models: Proposed Design Simulation Result

Supply Voltage (V)	CCMOS Power (uw)	Delay (PS)	Proposed Power(uw)	Delay
0.6V	0.8	40.8	0.38	43.4
0.8V	1.1	54.6	0.54	40.3
1V	1.28	60.3	0.85	38.5

3.3 Introduction to Cadence Tool

Cadence is a renowned EDA and semiconductor IP company. cadence allows engineers to produce the standard cells, IP blocks, and transistors needed in SoCs using custom/analog tools. In the most recent semiconductor processing nodes, our digital technologies automate the creation of giga - scale, gigahertz SoCs and their verification. IC packaging and PCB tools may be used to design our Whole Boards and Subsystems. Cadence also has a developing IP portfolio for memory, interface protocols, and verification.

The user interface in Cadence is visual, including windows, forms, and menus.DFW's primary windows are as follows: The environment is controlled through the Command Interpreter Window (CIW). It also acts as a log window for many of the tools that may be startedfrom here. The Library Manager displays the design libraries and the many buildings foundinside them. The current design is displayed in the Design Window (DW). It is possible tohave more than one. DW opened simultaneously with various (or the same) tools.

TW (Text Window) displays text. It might be a requested log or report, or copy editor.

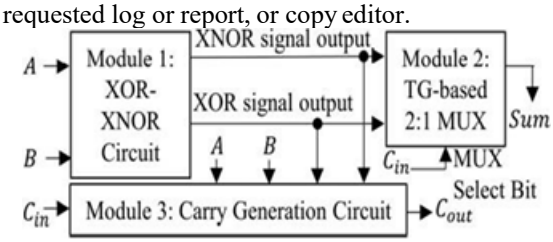

Figure 5. The design flow in cadence is as follows

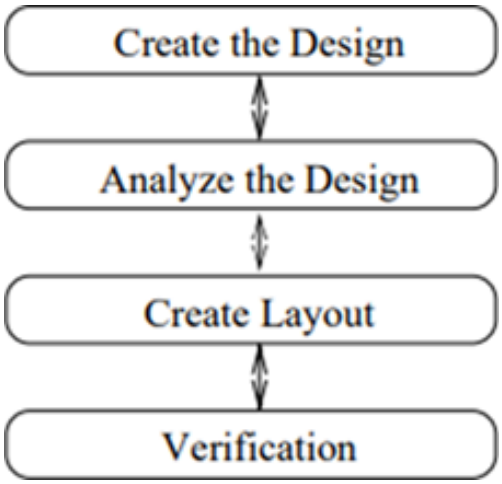

Figure .6. The design flow of cadence tool

4 PROPOSED DESIGNS

4.1 Design-1:

In this part, a brief explanation of the design of the XOR-XNOR-based hybrid full adder circuit's suggested block diagram is provided.

Here 3 blocks are combined together to form hybrid full adder circuit i.e., module-1 XOR-XNOR circuit, module-2 TG based 2:1 mux, module-3 carry generation circuit. And also, the output bits are A, B, Cin, and sum. It is composed of an XOR-XNOR module, a TG-based module, which produces the sum output, and a separate carry generating module, which takes input from the XOR-XNOR module and produces Cout output.

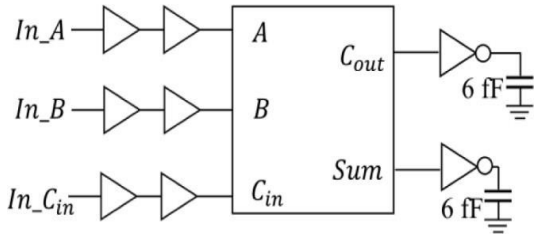

Figure.7 single bit full adder Simulation Test bench.

The FINFET-based transmission gates are used in the design-II schematic illustrated inFigure 7. For the proposed XOR circuit, the following requirements must be met.

Conditions:

I: If A = 0 and B = 0, then XOR = B=0 (since B = 0).

II: If A = 0 and B = 1, then XOR = B = 1 (since B = 1).

III: If A = 1 and B = 0, then XOR = A=1 (since A = 1).

IV: If A = 1 and B = 1, XOR = Gnd.

P5 and p6 switch on permitting weak logic 0 to go in the direction of the XOR node for requirement 1 of the formation of an XOR signal (since PMOS passes weak logic 0). n6 has been utilized to tackle this problem and offer solid rationale. In condition 1, A = 0, and p7 isactivated. As a response, logic 1 is assigned to the intermediatenode I. This logic 1 of Inactivates n6, which sends strong logic 0 tothe XOR node (since NMOS passes strong logic 1).

Table. 2. operation Table of XOR circuit

Pattern no	Input sideA	b	Complete transistor path	transistor route without a full swing	output signal or logic on the output side
1.	1	1	n_6 and n_7	GND	GND=0
2.	1	0	p_6	A	A=1
3.	0	1	p_5	B	B=1

The suggested XNOR circuit is subject to the following

I: IfA = 0, and B = 0, then XNOR = Vdd.

II: If A = 0 and B = 1, XNOR = A.

III: If A = 1 and B = 0, XNOR = B.

IV: If A = 1 and B = 1, XNOR = B.

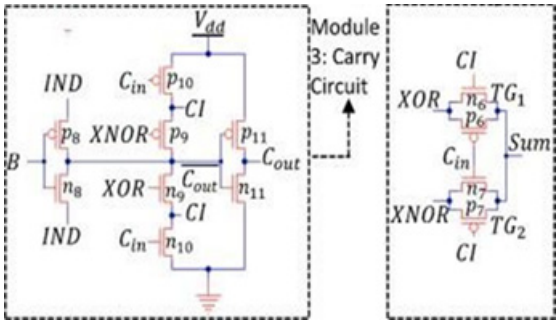

Figure. 8: Carry circuit

Table. 3: Operation Table of sum and carry circuits

Cin	Input pattern A	B	Cout	SUM
one	one	one	one	one
	one	zero	one	zero
	zero	one	1	0
	0	0	0	1
0	one	one	one	0
	one	o	0	one
	0	one	0	one
	0	o	0	o

If Cin = 0, Total = XOR (A XOR B).

If Cin = 1, Total = XOR (A XOR B) The Carrier Circuit's Conditions, If Cin is 0 then A=0 and B=0 then output will be Cout is 0 and sum is 0. Condition:2.If Cin is 0 then A=0 and B=1 then outputs will be Cout is 0 and sum is 1.condition:3. If Cin is 0 then A=1 and B=0 then outputs will be Cout is 0 and sum is 1.

V: If Cin is 0 then A=1 and B=1 then outputs will

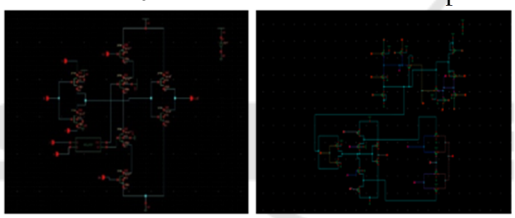

Figure 9: Depicts the NOR circuit's output

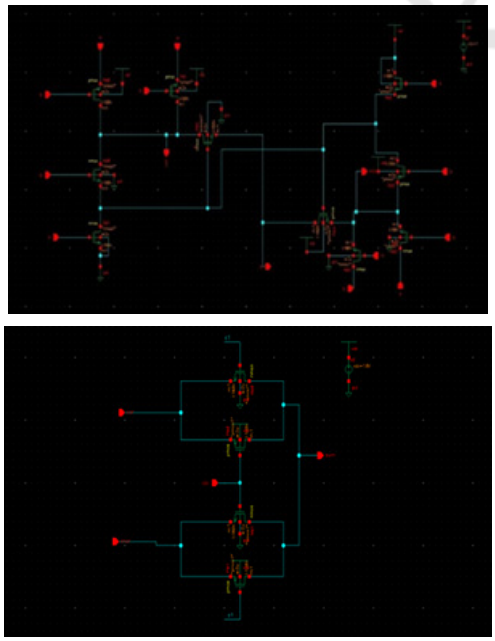

Figure 10: depicts the XNOR circuit's output

Figure 9 depicts the XOR circuit's output waveform. The same as explained in the table-4.1 of chapter-4. When the input logic is 0 0 for the XOR circuit then, the outputlogic is 0 and when the input logic is 01 or logic 10, then the output logic is always 1.And when the input logic is 11 then the output logic is always 0. waveform. is the same as explained in the table-4.2 of chapter-4. When the input logic is 0 0 for the XNOR circuit then, the outputlogic is 1 and when the input logic is 01 or logic 10, then the output logic is always 0. And when the input logic is 11 then the output logic is always 1.

5 RESULTS AND CONCLUSIONS

The scalable high-speed hybrid full adder based on XOR-XNOR gates' simulation results demonstrate how successful it is in terms of shorter propagation delays, lower power consumption, and compact design. These characteristics make it appropriate for energy-efficient and high-performance applications, particularly in digital circuits that need quick arithmetic operations.

An inventive idea in digital circuit design is a scalable, fast hybrid full adder architecture built on XOR-XNOR gates. These designs seek to maximize performance parameters that are essential for contemporary computer systems, such as speed, area, and power consumption.

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