# Design of a 1 to 4 Wilkinson Divider for 5G Mm-Wave Balanced Mixer

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Abstract:     In this paper, a 4 to 1 Wilkinson divider for a 5G mm-wave balanced mixer is presented. The proposed divider is studied and designed at 26 GHz using the PH15 technological process of UMS foundry. Simulation results, presented and discussed in this paper, are in good agreement with theoretical analysis. The 1 to 4 divider achieves good isolation, low reflection coefficients at all ports, and the minimum number of components. The divider is compact; it occupies 1.1mm*0.32mm, compared to the conventional one. Therefore, it can be easily integrated into a 5G mm-wave mixer.

## 1   INTRODUCTION

Integration promises reduced size, low power consumption, and reduced manufacturing costs of RF ICs, while simultaneously increasing system functionality and performance. However, the design of high-frequency integrated circuits and systems presents a significant challenge and requires adapting new architectures and design methods ((Es-saqy et al., 2020);(Es-saqy et al., 2021); (Didi et al., 2021); (Daghouj et al., 2020); (Boumaiz et al., 2019); (Moutaib et al. 2020); (Fattah et al., 2019);( Abdellaoui et al., 2019)). The performance of MMIC mixers has improved significantly with the development of high-performance transistors: pHEMT ((Huang et al., 2013); (Zhang et al., 2020)), HEMT (Hamada et al., 2020), CMOS ((Nam et al., 2020); (Gao et al., 2020)), and HBT (Song et al., 2020), and with the adaptation of new single- or double-balanced architectures. In most of these architectures, the use of a coupler/divider is indispensable.

In this article, a reduced dimension 1 to 4 power divider (or coupler) is studied and designed. It's inspired by the classic Wilkinson model (Kumar, 2019). However, it has an advantage over the latter, which has a reduced number of lumped elements to gain in terms of size. The reduced dimension 1 to 4 divider consists of four-phase shift cells. Comprising lumped components such as inductors and capacitors. Thus, we reduce the number of cells by two compared to the classical configuration, which had six cells (Xie et al., 2021).

To validate our 1 to 4 power divider design, we first proceed to matrix analysis. Then, we confirm this analysis by simulations in ADS software, validate the divider's design model, and integrate it in any MMIC circuit, in particular, double balanced mixers.

The paper is organized as follows: matrix analysis and circuit design are provided in Section 2. Section 3 presents the simulation results and discussion. Finally, concluding remarks are given in Section 4.

## 2   DESIGN OF A 1 TO 4 WILKINSON DIVIDER

As shown in Figure 1, the reduced-size 1 to 4 divider has four phase delay cells with four capacitors, four

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resistors, and eight inductors. These passive elements, whose behaviour is very close to reality, belong to the PH15 technological process from UMS foundry. We remind that all the ports of the divider are matched and loaded by Z0 impedances.

## 2.1 Matrix study of the reduced divider

Consider $S_{5*5}$ as the Wilkinson divider matrix:

$$S_{5*5}=\begin{pmatrix} S_{11} & S_{12} & S_{13} & S_{14} & S_{15} \\ S_{21} & S_{22} & S_{23} & S_{24} & S_{25} \\ S_{31} & S_{32} & S_{33} & S_{34} & S_{35} \\ S_{41} & S_{42} & S_{43} & S_{44} & S_{45} \\ S_{51} & S_{52} & S_{53} & S_{54} & S_{55} \end{pmatrix} \quad (1)$$

To simplify this matrix, we are interested in the particular characteristics of the 1 to 4 divider:

- Impedance matching: to minimize the reflections present on each port of the 1 to 4 divider, the divider must be matched to the load Z0 present on each of its five ports. Thus, all the terms present on the diagonal of the $S_{5*5}$ matrix are zero, i.e., $S_{11}=S_{22}=S_{33}=S_{44}=S_{55}=0$

- Isolation: the divider must ensure a good level of isolation between each of these four output channels, i.e., $S_{23}=S_{32}=S_{24}=S_{42}=S_{25}=S_{52}=S_{34}=S_{43}=S_{35}=S_{53}=S_{45}=S_{54}=0$

- Symmetry: the direct transmission parameters are identical to the reverse transmission parameters and are all equal, i.e., $S_{21}=S_{31}=S_{41}=S_{51}=S_{12}=S_{13}=S_{14}=S_{15}$

According to these three conditions, the $S_{5*5}$ matrix obtained is:

$$S_{5*5}=\begin{pmatrix} 0 & S_{21} & S_{21} & S_{21} & S_{21} \\ S_{21} & 0 & 0 & 0 & 0 \\ S_{21} & 0 & 0 & 0 & 0 \\ S_{21} & 0 & 0 & 0 & 0 \\ S_{21} & 0 & 0 & 0 & 0 \end{pmatrix} \quad (2)$$

The role of this circuit is the division by four of the power injected at the input, which results in a division by $\sqrt{4}$ of the amplitude. Consequently, the transmission parameters from the input to the outputs must have a modulus of a value of 1/2.

On the other hand, a signal injected at the input passes through four identical -90° phase shift cells. Therefore, a phase shift of -90° between the injected signal and the signal recuperated on one of the output

ports. A factor translates this phase shift -j. Therefore, the matrix S of the 1 to 4 divider becomes:

$$S_{5*5}=\begin{pmatrix} 0 & \frac{-j}{2} & \frac{-j}{2} & \frac{-j}{2} & \frac{-j}{2} \\ \frac{-j}{2} & 0 & 0 & 0 & 0 \\ \frac{-j}{2} & 0 & 0 & 0 & 0 \\ \frac{-j}{2} & 0 & 0 & 0 & 0 \\ \frac{-j}{2} & 0 & 0 & 0 & 0 \end{pmatrix} \quad (3)$$

Thus, by similarity with the classical three-port Wilkinson (Kiither et al., 1995), we can deduce that: $Z_L=2*Z_0$

We deduce from this that the following equation can express the values of the passive elements constituting the circuit:

- For the capacitors: $C = \frac{1}{2.w.Z_0}$
- For the inductances: $L = \frac{2.Z_0}{w}$
- For the four resistors: $R = Z_0$, this value allows better isolation between all the accesses.

## :2.2 Circuit Design

The electrical circuit is shown in figure 1. The divider is compact; it occupies 1.1 mm*0.32 mm. In contrast, the layout of the circuit is presented in figure 2. It shows that the capacitors have been removed. This is due to the low value of their capacitance (a few fF at 26 GHz). At this frequency, the parasitic capacitances of the inductors and the transmission lines have values in the order of those necessary for the operation of the coupler.
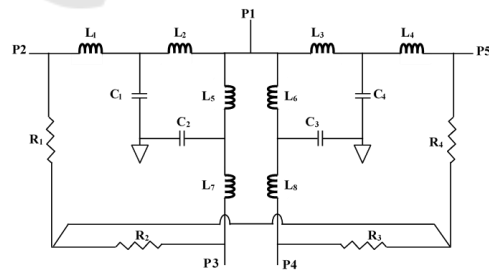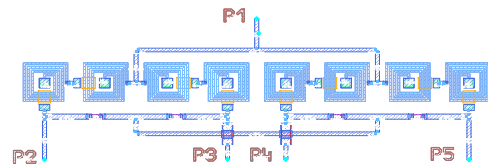


Figure 1: Reduced power divider circuit.



Figure 2: Reduced power divider Layout.

## 3 POST-LAYOUT SIMULATION

To validate our design method, simulations of the S-parameters of the circuit are carried out under Agilent's ADS software. These simulations are performed after the layout design; thus, the parasites related to the conduction lines are considered.

### 3.1 Reflection coefficients

A first simulation consists of checking the impedance matching of the five ports at 26 GHz. Figure 3 shows that at 26 GHz, the reflection coefficients are minimal. Since this circuit is designed using passive elements whose behaviour is very close to reality, these reflection coefficients are very low, less than -28 dB for S11. Thus the simulation results confirm our previous matrix analysis.
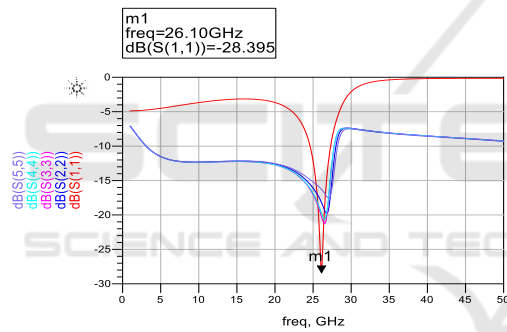
Figure 3: Reflection coefficients at the input and output of the four-way power divider.

### 3.2 Isolations

The second factor to check for validating our analysis of the 1 to 4 Wilkinson divider is the isolations between the different output ports. As the circuit has four output ports, we distinguish twelve terms that combine all these accesses.

The curves in Figure 4, showing the isolations between the different output ports of the divider. We can see that at 26 GHz, the isolation reaches its maximum level; S-parameters of minimum values reflect this. In the worst case, the isolation between ports '4' and '5' exceeds 15 dB, while the isolation between the other ports is more significant than 23 dB.
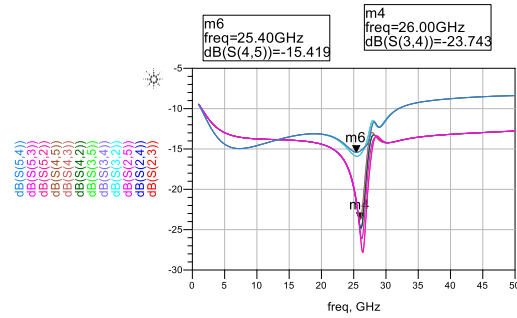
Figure 4: Isolation coefficients between outputs of the reduced four-way power divider.

### 3.3 Direct transmission coefficients

The direct transmission coefficients of the system are presented in figure 5, these coefficients reaching a maximum of -6.8 dB at 26 GHz. This maximum value confirms the division by four of the power injected at the input of the circuit and its distribution on all the circuit outputs.
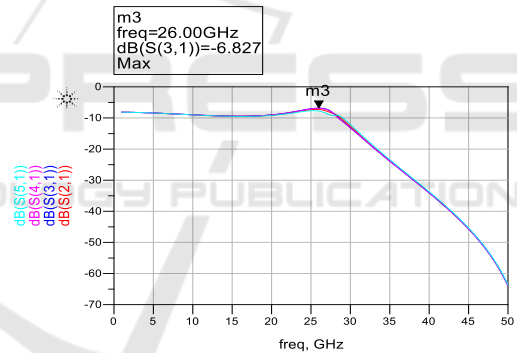
Figure 5: Direct transmission coefficients (from input to all outputs) of the reduced four-way power divider.
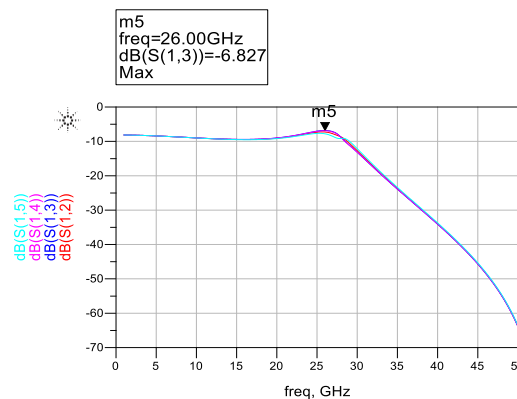
Figure 6: Inverse transmission coefficients (from outputs to all input) of the reduced four-way power divider.

## 3.4 Inverse transmission coefficients

The last validation step of our analysis consists of checking the reciprocity of the 1 to 4 divider circuit. For this purpose, the inverse transmission coefficients are shown in figure 6. These curves are identical to the curves of the direct transmission coefficients, which fully validates the matrix analysis presented before.

## 4 CONCLUSIONS

This paper has presented and designed a 1 to 4 Wilkinson divider for 5G mm-wave mixers. The divider achieves the performance of good isolation, low reflection coefficients at all ports, and good compactness, which make it suitable to be incorporated into double-balanced mixers operating in 5G mm-wave around 26 GHz. In our upcoming work, the circuit studied and designed in this paper will be integrated into a double-balanced up-conversion mixer.

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