Junction Temperature Measurement in Optically-Controlled Power Mosfet

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Abstract: The temperature-dependent optical properties of silicon carbide (SiC), such as refractive index and reflectivity, have been used for a direct monitoring of the junction temperature of a power MOSFET. In particular, the optical response of a 4H-SiC MOSFET-integrated Fabry-Perot cavity to temperature changes has been investigated through parametric optical simulations at the wavelength of 450 nm. The reflected optical power exhibited oscillatory patterns caused by the multiple beam interference for which the MOSFET epilayer, between the gate-oxide and the doped 4H-SiC substrate, acts as a Fabry-Perot etalon. These results were used to calculate the refractive index change and, therefore, the optical phase shift of $\Delta\varphi = \pi/2$ corresponding to a temperature variation that can be considered as a warning for the device "health". In practical applications, the periodic monitoring of the optic spectrum at the interferometric structure output gives an essential information about the device operating temperature condition that, for high power operations, may lead to device damages or system failure.

1 INTRODUCTION

The thermal control of any semiconductor device is of extreme importance to achieve optimal performance, reliability and durability. Temperature has a strong influence on the main electrical parameters and, for power devices or more complex electronic modules, in particular, a thermal management during the operating lifetime is exploited as a damage indicator to prevent the system failure.

In general, the thermal resistance of a device, R_T, is given by: $R_T = \Delta T/P$, where ΔT is the rise in temperature with respect to a specified reference point, and P is the power dissipated by the device. Ideally, the thermal resistance is a device specification that permits the user to determine the maximum temperature for any power level. In order for a device manufacturer to specify and, for a user to verify R_T, an accurate, reliable method for measuring the device internal temperature is required (Blackburn & Berning, 1982).

The technology of silicon carbide (SiC) is today recognized to be one of the most practical for pulsed-power applications taking, moreover, advantage from the high thermal conductivity of SiC which lowers the thermal resistance for a given active area and current density (Mazumder & Sarkar, 2009; Della Corte, Giglio, Pangallo, & Rao, 2018).

4H-SiC-based switching devices, in particular, can operate at high voltages and high currents up to theoretical temperatures higher than 800°C (Neudeck, 2006), however, the maximum allowed operating temperature of commercialized SiC-MOSFETs is usually lower than 175°C, limited by metals contacts, passivating materials and packaging technology (CREE, 2019).

Therefore, a continuous monitoring of the device junction temperature *(T_j)*, with a minimum of interference from the other device parameters, is

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essential to verify the power device "health" and to prevent damages.

In literature, many methods have been proposed for monitoring the power MOSFET temperature; these can be divided in three main categories (Blackburn, 2004): optical, physical contact and electrical methods. The main solutions use luminescence (Schuermeyer et al., 2000), Raman spectroscopy (Kuball et al., 2002), liquid crystals thermographic (Parsley, 1991), turn-on delay of impulse signal (Shi et al., 2017) or an external temperature sensor (Rao, Pangallo, & Della Corte, 2015).

However, each of these approaches only provide a global temperature whose value differs greatly from the real device junction temperature, T_j.

Recently, the linear relation between the body-drain voltage of power MOSFETs and their junction temperature has been experimentally investigated by these authors in a wide range of bias currents in a temperature range from about 22 up 150 °C (Pangallo, Rao, Adinolfi, Graditi, & Della Corte, 2019). Moreover, a new method for measuring the T_j of power light emitting diodes (LEDs), used for lighting, has been presented (Pangallo et al., 2018) together with a microcontroller-based circuit designed and realized for a real-time monitoring (Della Corte et al., 2020).

In this work, we present a new approach allowing the junction temperature control of a 4H-SiC power MOSFET through an optical signal. Optical simulation results of the MOSFET-integrated Fabry-Perot cavity, consisting of the gate oxide, the epilayer and the doped substrate, show that the temperature-induced refractive index change allows to calculate the T_j variation. The proposed optically-controlled power MOSFET junction temperature can be done during the lifetime of the device in order to alert the user before its failure.

2 DEVICE STRUCTURE AND SIMULATION RESULTS

A 4H-SiC-based MOSFET structure has been modeled using R-Soft CAD (RSoft, 2006), a photonic device simulator using the beam propagation method, to perform 3-D parametric optical simulations.

The MOSFET-integrated Fabry-Perot cavity, in the <x,z> plane, where <z> is the optical propagation direction, is shown in Figure 1. Simulations were performed using a continuous laser optical beam, at the wavelength of 450 nm, launched on top of the gate-oxide layer. Layers thickness and optical data of the materials used for simulations are listed in Table 1.

As shown in Figure 1, the optically-controlled MOSFET has an optical window instead of the gate electrode. When the light falls on it, no excess carriers, at the considered wavelength of 450 nm, are generated, therefore, the conductivity as well as the drain current are not influenced by the optical signal used for the device temperature monitoring. It is worth noting that the control of T_j is generally done using a short pulse laser source with a repetition rate comparable or lower than the slow thermal dynamics of the device.

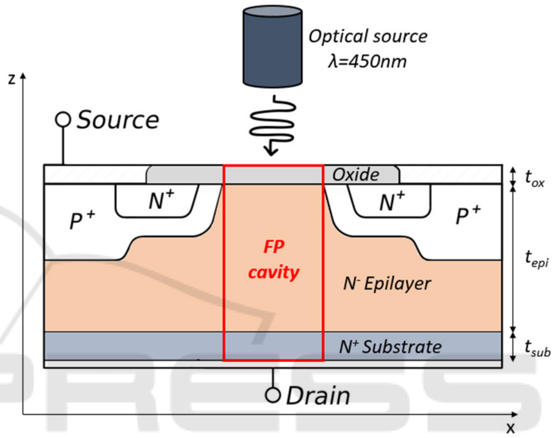

Figure 1: Schematic cross-section of an optically-controlled 4H-SiC MOSFET. The MOSFET-integrated FP cavity consists of the 4H-SiC epilayer between the SiO_2 gate-oxide and the 4H-SiC heavily-doped substrate.

Table 1: Optical and geometrical parameters of the MOSFET-integrated FP cavity.

Silicon oxide thickness (t_{ox}) [µm]	0.1
Channel length [µm] (Della Corte, De Martino, Pezzimenti, Adinolfi, & Graditi, 2018)	6.5
Epilayer thickness (t_{epi}) [µm]	10
Substrate thickness (t_{sub}) [µm]	2.5
Silicon oxide refractive index (n_{ox})	1.44
Epilayer refractive index (n_{epi}) (Watanabe, Kimoto, & Suda, 2012)	2.73
Substrate refractive index (n_{sub}) (Lim, Manzur, & Kar, 2011)	2.65

From a technological point of view, the power MOSFET fabrication requires a high quality of both epilayer surfaces, therefore careful attention towards the morphology of all stacked-layers is performed in any industrial process. Optical microscopy (OM) is a fast and non-destructive method, which is generally used after each growth to determine the morphology, uniformity and epilayer defects (Ager III, 1998). Moreover, OM is carried out also to reveal any presence of 4H-SiC domains when the growth is performed on doped-SiC substrates.

Under these technological conditions, a reflectance spectrum can be registered at the input of the Fabry-Perot (FP) cavity consisting of the smoothed gate-oxide/epilayer and epilayer/substrate interfaces.

The interference fringes are detected, in case of homoepitaxy, as in our structure, due to a difference in refractive index between the epilayer and the substrate (see Table 1). This difference is achieved by the strong doping concentration discrepancy between the 4H-SiC epilayer (N_D-N_A ~10^{16} cm^{-3}) and the 4H-SiC substrate, which has usually a nitrogen doping concentration in the range 10^{18}-10^{19} cm^{-3} (Della Corte et al., 2018).

Figure 2 shows the simulated FP reflected spectrum centered at the wavelengths of interest. The corresponding calculated Free Spectral Range *(FSR)* is 3.57 nm, in agreement with the theoretical value (Agrawal, 2012).

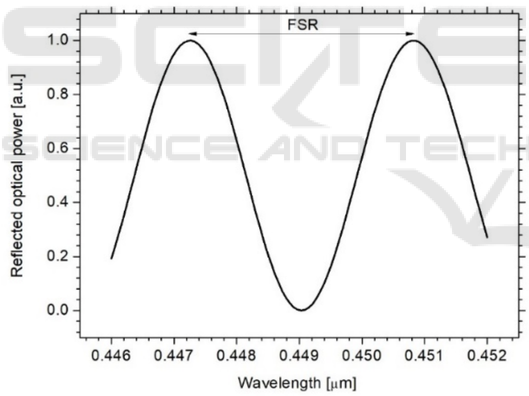

Figure 2: Normalized-reflected output power *vs.* wavelength. The *FSR* is the spacing in wavelength calculated between two successive reflected optical intensity maxima (or minima) of the FP cavity.

For the refractive index values considered in this work (n_{sub}=2.65, n_{epi}=2.73), the modulation depth, defined as $M_{\%} = (I_{MAX} - I_{MIN}) / I_{MAX}$, where I_{MAX} and I_{MIN} are the maximum and minimum intensities of the reflected signal, is 15.2%, varying from $M_{\%}$=24.2% down to $M_{\%}$=5.4% for n_{sub}=2.6 and n_{sub}=2.7, respectively.

Moreover, parametric simulations were performed in order to verify the independence of the gate oxide thickness, considered in this work from 50 to 500 nm, on the FP outputs. The used value of 100 nm is typical for commercial power MOSFETs.

As known, the temperature dependence of the optical path length of a monochromatic light, incident perpendicularly upon a device surface and traveling through a FP cavity, is given by the product between the refractive index of the cavity material, *n*, and its length, *L* (Steimacher et al., 2004).

Due to the environmental and/or operating conditions, a variation of the temperature, ΔT, induces both *n* and *L* change and, therefore, the optical length changes too, as well as the interference phase angle of the oscillatory pattern, φ, as expressed by the following equation (Mathew et al., 2015):

$$\frac{\Delta\varphi}{\Delta T} = \frac{4\pi n L}{\lambda}\left[\frac{1}{n}\frac{dn}{dT} + \frac{1}{L}\frac{dL}{dT}\right] \quad (1)$$

where *dn/dT* and *dL/dT* are the thermo-optic *(TOC)* (Faggio, Messina, Gnisci, Rao, & Malara, 2019) and the thermal-expansion coefficients, respectively.

In our structure, the MOSFET-integrated FP cavity length is the epilayer thickness, t_{epi}, and the corresponding refractive index is n_{epi}. A phase shift of $\Delta\varphi = \pi/2$ results in a complete tuning of resonance wavelengths and, from equation 1, if we consider a *TOC* of $7.8 \cdot 10^{-5}$ at λ=450 nm (Watanabe et al., 2012), and $dL/dT = 2.2 \cdot 10^{-6}$ (Nakabayashi, Fujimoto, Katsuno, & Ohtani, 2006), the theoretical temperature change is expected to be $\Delta T_{\pi/2}$ =133.92°C.

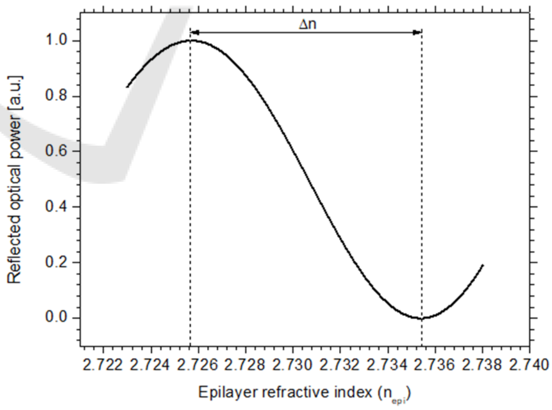

Figure 3: Reflected output power *vs.* epilayer refractive index. The difference of refractive index between a maximum and a minimum value of the refrected power is $\Delta n = 9.65 \cdot 10^{-3}$.

Figure 3 shows the parametric simulation results of the MOSFET-integrated FP cavity spectrum where the epilayer refractive index has been varied in a range allowing a gradual and complete detuning of the cavity, e.g., from a maximum to a minimum of the reflected power at the gate-oxide output.

Assuming for 4H-SiC a TOC of $7.8 \cdot 10^{-5}$, it can be calculated that a complete FP detuning is introduced in our L=10 µm-thick 4H-SiC epitaxial layer by a thermally-induced refractive index change of $\Delta n = 9.65 \cdot 10^{-3}$ corresponding to a temperature variation of $\Delta T_{\pi/2}$=123.7°C.

It is worth noting that this temperature variation mainly depends on the wavelength of the optical signal and/or on the MOSFET epilayer thickness. However, if the optical parameters, at a specific wavelength, as well as the MOSFET geometry, are not known, an easy pre-characterization of the MOSFET-integrated FP cavity spectrum allows the determination of the temperature change ($\Delta T_{\pi/2}$) required for the output optical power to move from a maximum (or minimum) to a subsequent minimum (or maximum).

In a practical application, if we consider, e.g., an external temperature of T_e=30°C, the monitoring of the multiple-beam interference signal, from its resonance position, gives us the power device/system operating temperature condition ($T=T_e+\Delta T$) that, for high power operations, in particular, may lead to permanent damage or performance variations.

3 CONCLUSIONS

In this paper, a new method for real-time monitoring the junction temperature of a SiC-based power MOSFET has been presented.

The MOSFET epilayer between the gate-oxide and the heavily doped substrate naturally forms an integrated Fabry-Perot (FP) cavity that can be exploited to calculate the temperature variation during the power device operating life.

Simulation results, performed at the wavelength of 450 nm, showed that a complete FP detuning is introduced in our L=10 µm-thick 4H-SiC epitaxial layer by a thermally-induced refractive index change of $\Delta n = 9.65 \cdot 10^{-3}$ corresponding to a temperature variation of 123.7°C. The optically-controlled junction temperature increase is essential to prevent the device overheating.

This method can be applied in many power applications, including signal-conditioning circuits for sensors (Rao, Pangallo, & Della Corte, 2016), and for wide-band materials-based switching system control where, changes in temperature above the temperature limit, lead to a mean time to failure reduction or device disruption.

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