A 0.13 μm BiCMOS Reconfigurable Analog Baseband for Multi-mode Multi-standard Wireless Receivers

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Keywords: Analog Baseband (ABB), Reconfigurable, Multi-mode Multi-standard, BiCMOS.

Abstract: This paper presents a reconfigurable analog baseband (ABB) for multi-mode multi-standard wireless applications. By having digitally controllable transconductance and transimpedance amplifier stages, the gain, noise figure (NF) and linearity of the analog baseband can be reconfigured. Fabricated in IBM 0.13 μm BiCMOS process, the analog baseband achieves voltage gain from 4.4 to 33.3 dB. Simulated maximum input 1-dB compression point and input intercept point (IIP3) are 1.2 dBm and 11.2 dBm respectively. Simulated minimum noise figure is 9.4 dB. The current consumption for a single branch (I or Q) ranges from 3.5 to 4.5 mA from 1.8 V supply voltage. The chip occupies an area of 0.2 mm².

1 INTRODUCTION

Recently, various kinds of wireless applications for handset mobile terminals are emerging and industries are making great effort to enable mobile terminals to support all functionalities related to various existing and new born communication standards. It is hoped that, those mobile terminals, with low price and low power consumption, can provide us high-quality services including long distance communications (e.g., TD/FD-LTE, WCDMA, GSM, Satellites) and short range communications (e.g., WLAN, WPAN, UWB) (Lin et al., 2015). It is necessary to design a receiver, which is compatible with multiple communication standards.

Software defined radio (SDR), which is innovated to use digital receiving and transmitting instead for analog processing of signals (Abidi, 2007), provide us a new way to realize the integration of different function in one terminal. However, SDR put so stringent requirement on analog to digital converters (ADC) that it can hardly be realized nowadays. An evolved SDR architecture can be used to organize a receiver, which is essentially a reconfigurable zero intermediate frequency receiver as shown in Fig. 1. This receiver can be tuned to any carrier frequency, with any signal bandwidth, any modulation fashion. The flexible reconfigurability requires that every circuitry block of the receiver should be reconfigurable.

One of the key building blocks for multi-mode multi-standard receiver is the analog baseband (ABB) circuit, which consists of a transconductor stage and a transimpedance (TIA) stage. The gain of the ABB should be reconfigurable to provide several degrees of freedom. Some ABBs have been proposed (Kwon and Han, 2014; Hedayati et al., 2015), however, the gain cannot be tuned and the receiver could be blocked by interference signals. In this paper, we present an ABB with a bias circuit. The ABB can be flexibly reconfigurable in terms of gain, which is a great advantage for multi-mode multi-standard receiver.

The paper is organized as follows: The reconfiguration arrangement and design considerations for ABB are presented in Section 2 and 3. Simulated results are shown in Section 4. Finally, conclusions are drawn in Section 5.
2 RECONFIGURATION ARRANGEMENT

The block diagram of the reconfigurable ABB is illustrated in Fig. 2. The proposed ABB includes symmetrical I/Q branches and bias cell. Each of I and Q branches is composed of a reconfigurable transconductor stage and a reconfigurable TIA stage.

3 DETAILED CIRCUIT DESIGN

In this section, the circuit design of the analog baseband shown in Fig.2 is presented in detail.

3.1 Bias Circuit

A better performance can be obtained by using a constant transconductance bias circuit. As shown in Fig. 3, the whole circuit DC bias points are provided by a proportion to absolute temperature (PTAT) bias network for BJT and a temperature compensation (TC) bias network for MOS to ensure constant transconductance. The bias current are given (Razavi, 2001):

\[ I_{PTAT} = \frac{2V_T \ln \left( \frac{A_{Q2}}{A_{Q6}} \right)}{R_3} \]  

(2)

\[ I_{TC} = \frac{2V_T \ln \left( \frac{A_{Q2}}{A_{Q1}} \right)}{R_1} + \frac{V_{be,Q1} + V_{be,Q4} - V_{be,Q5}}{R_2} \]  

(3)

where \( V_T \) is the thermal voltage, \( A \) is the emitter area of bipolar transistor, and \( V_{be} \) is the base-emitter voltage of bipolar transistor.

3.2 Transconductor Stage

The schematic of the reconfigurable transconductor stage is illustrated in Fig. 4. The input DC voltage is very low (e.g., 0.3V) for reducing the on-resistance of the mixer, so the level shift circuit is necessary to offer an appropriate DC point. The transconductor stage is the combination of a fixed transconductor and a \( V_C \)-controlled transconductor. The fixed transconductor are provided by MOS transistors \( M_1 \) and \( M_2 \). The source negative feedback resistors \( R_7 \) and \( R_8 \) can further increase linearity. The other parallel branch is consisted by BJT \( Q_1 \) and \( Q_2 \), which can offer a lager transconductance. NMOS switch is used to control on and off of the BJT branch, PMOS switches are used to maintain the output operating point stable.

3.3 TIA Stage

TIA works as a current amplifier and converts...
current signal to voltage signal at output. The TIA also provides some low-pass characteristic for channel selection and interference attenuation. The transimpedance is determined by the feedback resistor $R_{TIA}$. The reconfigurable gain is realized by paralleling the resistors, as shown in Fig. 5.

The cut-off frequency is depended on the $R_{TIA}$ and the feedback capacitor $C_{TIA}$:

$$\omega_0 = \frac{1}{R_{TIA}C_{TIA}}$$  \hspace{1cm} (4)

$R_{TIA}$ and $C_{TIA}$ are controlled by two opposite control words to make their product is unchanged. So the bandwidth does not change with various gains.

The operational transconductance amplifier (OTA) with a high gain-bandwidth (GBW) is necessary to reduce the input impedance of the TIA which can be close to zero in a wideband. This paper adopts a 2-stage miller-compensated OTA (Willy, 2006) which is depicted in Fig. 6. This fully-differential amplifier uses four equal resistors ($R_{C1} - R_{C4}$) to cancel out the differential signals and offer the common-mode biasing voltage.
4 LAYOUT AND POST-SIMULATED RESULTS

The layout of the whole ABB by using IBM 0.13μm BiCMOS process is shown in Fig. 7. The overall area is 0.57μm × 0.36μm. The supply voltage of the chip is 1.8V and the power consumption is 14.2/17.8 mW (without output buffer).

![Layout of the baseband circuit.](image)

Figure 7: Layout of the baseband circuit.

Fig. 8 illustrates the post-simulated of voltage gain curves with various $G_m$ and different size of $R_{TIA}$. 4 gain steps (34.3/28.3/10.4/4.4 dB) are clearly shown to meet different applications.

![Post-simulated of gain curves with different $G_m$ and $R_{TIA}$.](image)

Figure 8: Post-simulated of gain curves with different $G_m$ and $R_{TIA}$.

The ABB has the minimum NF of 9.4 dB at the highest gain mode as shown in Fig. 9. And it has best linearity under the lowest gain mode. The highest post-simulated IIP3 is about 11.2 dBm with two-tone signals $f_{IF1} = 1.06MHz$ and $f_{IF2} = 1MHz$ as shown in Fig. 10.

![Post-simulated of NF under the highest gain mode.](image)

Figure 9: Post-simulated of NF under the highest gain mode.

![Post-simulated of IIP3 under the lowest gain mode.](image)

Figure 10: Post-simulated of IIP3 under the lowest gain mode.

Tables 1 summarize the measured results of the proposed reconfigurable baseband circuit and give a comparison with other recently published works. The comparison indicates that the proposed analog baseband exhibits wide-controllable gain range, low noise figure and good linearity performance.

5 CONCLUSION

This paper presents a reconfigurable analog baseband (ABB) circuit for multi-mode multi-standard wireless receivers. The reconfiguration arrangement and block design considerations are described. The design concept is verified by implementing in IBM 0.13μm BiCMOS process.
Table 1: Performance comparison.

|                     | This Work | ASICON  
(Jiachen, Zheng, and 
(Fan, Tao, Bao, and 
Wang, 2016) | TMTT 
(Namsoo, Vladimir, 
and Lawrence, 2010) |
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<tr>
<td>Technology</td>
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<td>65nm CMOS</td>
<td>0.18 μm CMOS</td>
<td>0.18 μm CMOS</td>
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<tr>
<td>Gain (dB)</td>
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<td>22.5–25</td>
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<td>Bandwidth (MHz)</td>
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<td>4</td>
<td>12</td>
<td>NA</td>
</tr>
<tr>
<td>Min Noise Figure (dB)</td>
<td>9.4</td>
<td>30.7</td>
<td>9</td>
<td>8</td>
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<tr>
<td>IIP3 (dBm)</td>
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<td>-27(58dB)</td>
<td>9</td>
<td>7</td>
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<tr>
<td>Supply Voltage (V)</td>
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<td>1.2</td>
<td>1.8</td>
<td>2</td>
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<tr>
<td>Bias current (mA)</td>
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<td>1.9–2.1</td>
<td>8.2–13.2</td>
<td>5</td>
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<tr>
<td>Note</td>
<td>Gm+TIA</td>
<td>Gm+TIA</td>
<td>Gm+mixer +TIA</td>
<td>Gm+mixer +TIA</td>
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The ABB can achieve 4 gain steps, high linearity and low noise performance at the desired gain mode. The proposed ABB provides a good alternative in the applications of multi-mode multi-standard wireless communications.

ACKNOWLEDGEMENTS

This paper is supported by the National Basic Research Program and the Priority Academic Program Development of Jiangsu Higher Education Institutions. And we are grateful for the encouraging discussions and technique assistances of the whole team in Institute of RF- & OE-ICs, Southeast University.

REFERENCES


