A NOVEL DESIGN AND DEVELOPMENT OF A SINGLE CHANNEL INTEGRATED DIGITAL BODY SOUND DATA ACQUISITION DEVICE

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Abstract: This paper discusses the design, development, and testing of an integrated compact digital stethoscope capable of performing body sound measurement and processing without the need of a personnel computer and hardware interface. The cost of the proposed device is a fraction of that of the data acquisition system used with current digital stethoscopes to collect body sound, such as lung sound, in a digital format. Preliminary testing of the device shows faithful reproduction of the body sound signals used. Not only the new design strategy saves hardware, space, and power consumption but also it allows for the signal processing and data interpretation in the same device. This is due to the proposed integrated design of the subsystems involved in the data acquisition process. It also has the capability of sending collected data to remote location through the Internet.

1 INTRODUCTION

Auscultation is the most popular method for the diagnosis of pulmonary dysfunction. The breath sound that originates in the lungs was first subjectively acquired by a stethoscope and it is at present the most effective mechanism for the analysis of lung sounds by human audition. Lung sounds are used to detect diseases such as the obstruction during bronchial provocation testing. They have drawn much attention because it does not require maximal breathing effort and can therefore be used with young and elderly patients (Oavriely, N., 1996). In recent years, the diagnostic power using auscultation has significantly improved because of the advances in data acquisition, digital signal processing and signal analysis. (Cohen, A. and Landsberg, D., 1984)(Cohen, A., 1986)(Druger, O., 1973)(Hartman, X., 2001)(Kiyokawah, H., Yonemarum, M., Horie, S. et al, 1995)(Kraman, S.S. and Austrheim, D., 1983)(Lehrer, S., 1989)(Urquhart, R.B., McGee, J., Macleod, J.E., Banham, S.W. and Moran, F., 1981)

Current digital measurement of body sound requires a personnel computer and a data acquisition system beside the stethoscope, see Figure 1. The current technology is cumbersome and expensive. The cost of the data acquisition card used by one of the authors, (Alouani, A.T. and A. Kamal, 2006), to collect digital lung sound was over $1,400 (National Instruments, 2007). Nowadays, handheld devices like Personal Digital Assistants, cell phones, and other handheld gadgets use sophisticated chip technology, which allows for lightweight, compact and very limited power consumption. Field Programmable Gate Array (FPGA) technology is currently used in these devices. Not only this technology consumes power in milli watts but also it allows the integration of processing power, on-chip memory and various control interfaces.

The objective of this paper is to design, implement, and test an integrated digital stethoscope capable of acquiring body sound in a digital format without the need of a data acquisition system or a personnel computer. Using the great computational power of modern FPGAs, the proposed device is capable of performing the desired signal processing and analysis of the lung sound. The total cost of the proposed body sound measurement and processing device is expected to be a fraction of that of the existing data acquisition system (National Instruments, 2007).

This paper is organized as follows: section 2 reviews the basics of the FPGA highlighting its capability for integration and compactness. Section 3 contains the conceptual design of the proposed body

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sound measurement device. Sections 4 and 5 discuss the hardware implementation and testing of the device. Then, section 6 contains the conclusions and discussions.

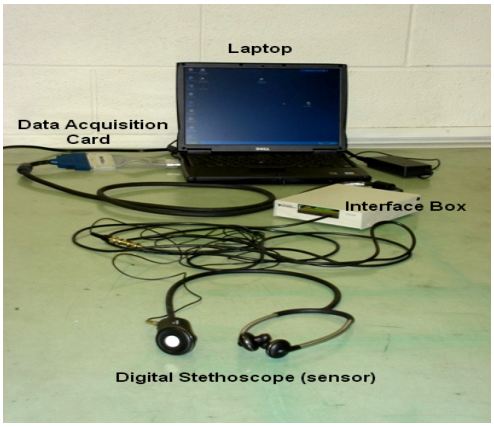

Figure 1: Digital Body Sound Measurement Using Current Technology.

2 FPGA OVERVIEW

FPGA is a programmable integrated circuit that is manufactured with high density of internal blocks. Typically, an FPGA is made up of digital signal processors (DSPs), configurable logic blocks (CLB), memory cells, input output blocks, and microprocessors (Xilinx Inc. 2007), see Figure 2. By configuring these blocks, the FPGA is capable of communicating with external peripherals, processing and storing data.

The FPGA is a stand-alone reconfigurable system-on-chip with the above capabilities. Using this FPGA technology, the development of new applications becomes very affordable. Examples of advanced commercial FPGA-based low cost battery operated handheld devices are Personal Digital Assistants (PDAs), cell phones, and MP3 players.

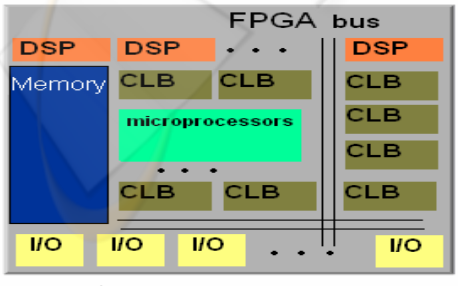

Figure 2: Advanced FPGA technology can have embedded memory, Central Processor, Digital Signal Processors (DSP), input/output (I/O) blocks, interconnects, and configurable logic blocks (CLB) in one chip.

3 CONCEPTUAL DESIGN

Existing computer based data acquisition systems, such as the portable digital stethoscope system shown in figures 1 or the portable EEG system (Comet®, 2007) shown in Figure 3, are complexes of many components. A general structure of such systems is shown in figure 4. The sensor(s) output is connected to a dedicated Analog/Digital (A/D) converter. The A/D converter sends data to a computer. The computer analyzes the acquired signals using its signal processing and decision making capabilities. The computer system contains programming memory, storage memory (i.e., hard disk) and is connected to the internet through its internal network interface card. Even though these systems are portable, they are quite cumbersome and expensive. In addition, their power consumption is much higher than that of handheld devices.

The cumbersomeness of existing portable medical data acquisition devices is due to the lack of integration and the reliance on a personal computer, Figure 3. The connections between the different subsystems require special cables and at times connection boxes, such as the one in Figure 1. On the other hand, the FPGA allows for the integration of various components on one chip. In addition, it has all the processing, storage and display capabilities needed by a medical data acquisition system. Finally the proposed device is Internet ready. This research provides a new design philosophy that takes advantage of the capabilities of the FPGA to eliminate the need of a computer and cable based connection between subsystems. This new design strategy is summarized in Figure 5.

Figure 3: Comet® portable EEG with, stimulator, and isolated power supply (Comet®, 2007).

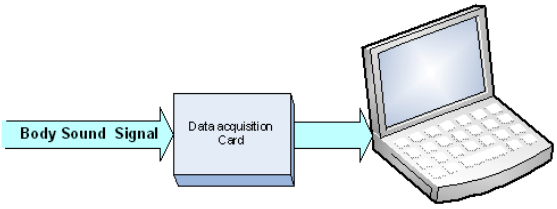

Figure 4: Existing Body Sound Data Acquisition System.

4 HARDWARE DESIGN AND IMPLEMENTATION

A centre piece of the proposed compact body sound data acquisition system is the FPGA. The FPGA communicates directly to the A/D converter. The proposed FPGA design includes an A/D configuration module, which issues configuration words containing desired A/D sampling rate, resolution, gain, etc. Also, the FPGA collects data from the A/D converter, via the Data Recording unit. Preliminary digital signal processing, such as power spectrum density computation and display can be done by the FPGA data processing unit. Writing the processed data into the Flash memory device takes more time than that of all operations preceding it. So, care is given to the design of the Data Recording unit, to avoid timing problems. It is advantageous to use the FPGA's internal memory cells for buffering because their access time is much smaller than that of external memories. However, FPGA's internal memories are limited. External off-chip memory is used to store the sound samples in a buffer of large blocks of data. As this buffer is filled, the write operation is performed for the entire buffer. This ensures the continuity of recorded data. The size of the whole buffer is set to sufficiently hold a contiguous useful data set from a body sound site. Of course, the maximum size of the buffer is limited by the size of the external memory. The Data Recording unit writes the collected data into the detachable external Flash memory device for further analysis. The Data Recording unit follows an error detection algorithm in the data writing process to ensure the integrity of the stored data.

Particularly, the FPGA writes acquired data after filling data buffer. In order to optimize the acquire-and-write processes, the Data Recording unit can use single or multiple block writing mechanisms. Data block writing uses an integrity check value (Cyclic redundancy check) at the end of each block. In multiple block writing, the total write time is reduced significantly by use of a more sophisticated write mechanism. The time reduction is important as it allows for fast A/D sampling rate. This will in turn improve the faithful reproduction of the acquired data.

4.1 Design Requirements

Mixed FPGA hardware/software architecture is employed using Hardware description language (HDL). As a rule of thumb, all time-critical tasks are implemented in hardware, while other functions are developed in software using embedded C programming language. For example, the software is used to process the captured data, while the hardware is used to configure the A/D converter, and provide proper timing signals. The FPGA bus signals and the parallel input output lines form a common interface between the hardware and the software components.

In traditional systems, Flash memories are written by a host personal computer, through a permanent interface (i.e. soldered chips on circuit boards). Such use of Flash memory devices is common in embedded systems to store configuration information.

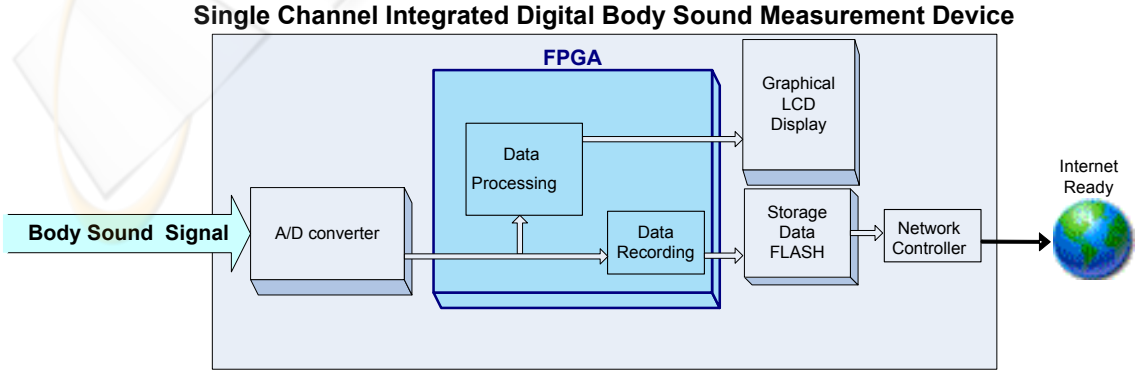

Figure 5: Proposed Integrated Body Sound Data Acquisition System.

One design choice made here is to use detachable Flash memory devices. Sampled data must be written to the Flash memory device to allow further remote analysis and interpretation. This introduces various technical design challenges. Particularly, Flash memory must be written by a customized hardware not by a personal computer. Hence, the proposed Compact Body sound Data Acquisition System must address the following design requirements.

4.1.1 High Data rate

A Detachable Flash memory should have a small and robust physical interface. This limits the maximum number of data and control pins in the interface. Consequently, this affects the writing speed, as serial data communication must be employed. We have used high clock frequency in serial mode to overcome this challenge. Timing and clock signals between the FPGA and the A/D converter are properly matched. We have used Phase Locked Loop (PLL), and clock dividers to achieve this matching.

4.1.2 Data Integrity

Flash memory must be initialized before the storing process. As Flash memory cards are detachable, card detection and initialization are required. The storing process can not be done unless the Flash memory is initialized. Continuous monitoring of the Flash memory during both the reading process and the writing process is done to ensure that the data is passed to the Flash memory. We have used Error check code to check the valid arrival and storage of the data into the Flash device.

4.1.3 Data Quality

The writing process is limited by the access time of the Flash memory device (typically 10 to 200 µs (Western Digital, 2007)). High quality data should be received fully (without dropped blocks), in proper order and in time. There is no need to store data which is incomplete or out of order. One solution we have used is to use internal buffer. We assume no data compression, and fixed data arrival rate. We have made sure that the processing rate is faster than the arrival rate. In future work, we will consider variable data arrival rate (e.g. compressed data), and will evaluate the optimal buffer depth, such that no blocks are dropped.

4.2 Design Implementation

Firstly, the Altera SoPC ™ builder is used to layout the contents of the FPGA; the NIOS-II processor, peripheral components and memory cells, as well as the custom hardware logic we have designed. The FPGA layout is compiled and mapped to the target device in the Altera Quartus environment. Finally, the NIOS-II integrated development environment (IDE) is used to design the software components of the FPGA.

The NIOS-II processor core is connected to rest of the FPGA components through the Altera Avalon bus interface. The Avalon interface contains the arbitration logic to manage various module connections (Altera Quartus II, 2006) (Sadik C. Esener, 2006). The NIOS-II processor is a 32-bit Reduced Instruction Set processor. Since the NIOS-II processor follows Harvard Memory architecture, the data and the program are stored on separate memories. It has a 4-KB instruction cache and a 2-KB data cache. The processor runs on 50 MHz clock frequency.

The A/D converter used in the proposed system is a WOLFSON WM8731. It can support a range of sampling frequencies from 8 KHz to 96 KHz. It has internal digital filters to improve the sound quality. Sound data is fed to the NIOS-II processor in FPGA serially (Altera DE2, 2006).

The proposed system stores body sound input signals in pulse code modulation using the Wave (.wav) file format (Bashir A., 2007)(Wolfson Microelectronics, 2006). The sound is stored as a 16-bit mono with a sampling frequency of 48 KHz.

5 EXPERIMENTAL TESTING

Figure 6 shows the proposed system prototype implemented using FPGA. The produced prototype uses only 15% of the total chip capacity that is 5114 out of the 33,216 Logic Elements of the Altera Cyclone-II EP2C35F672C6 FPGA chip. The worst-case prorogation delay observed for the system is 12.04 ns, which is less than the 50 MHz clock period of 20ns. The Cyclone-II FPGA consumes as low as 12 mW of power, which rivals semi-custom ASIC counterparts of similar cost.

Several tests have been performed using this prototype. We have used the existing computer based system to acquire a lung sound. The same signal was provided to the newly designed device, figure 6. Only the results of one experiment are reported in this paper.

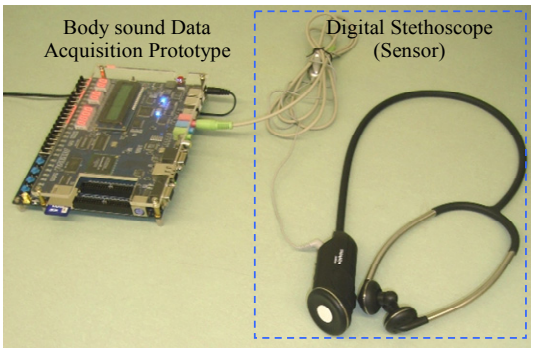

Figure 6: FPGA prototype of the Integrated Data Acquisition System.

The computer based system acquired the lung sound shown in figure 7. The experiment run length is 2.6 seconds (horizontal axis). Plotted on the vertical axis is the normalized signal amplitude. The data recorded using the proposed integrated data acquisition system is shown in figure 8. Figure 9 provides a zoomed in view to show the faithful reproduction of the body sound signal.

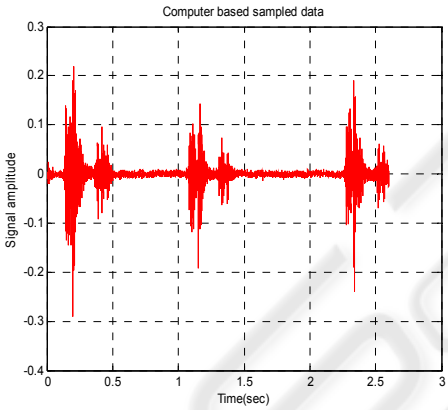

Figure 7: Data recorded using the existing Data Acquisition System.

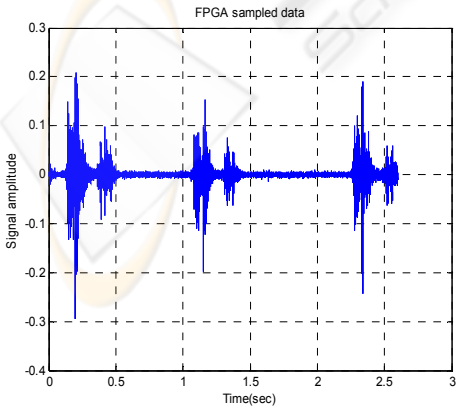

Figure 8: Data recorded using the proposed Compact Integrated Data Acquisition System.

6 CONCLUSIONS

This paper provided a new design philosophy of future integrated and compact medical data acquisition systems. The design takes advantage of latest development in the system-on-chip technology.

In this paper, the design, development, and testing of the body sound measurement device took place using the Altera development board. The design of an optimized custom board for this application is underway. The new board will eliminate components, such as off-chip-memory devices, extension header network ports, that are not needed by this device. In addition, the sound sensor (microphone) will be integrated in the new board. This will eliminate the need for the stethoscope, which in turns reduces the cost of collecting digital body sound.

This new design direction in medical data acquisition systems saves hardware, power consumption, and more importantly money. Future work will focus on developing universal medical data acquisition systems using the design philosophy reported in this paper. It is believed that the long term benefit of this research will provide affordable handheld medical data acquisition systems with remote data transfer capability. This will in turn make health screening affordable and feasible from the patient location.

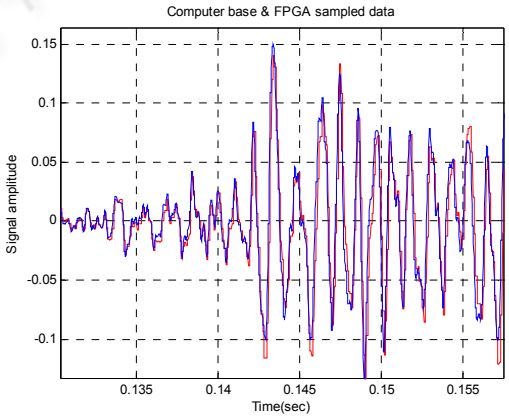

Figure 9: (Time zoom) Superimposed Data recorded using both Data Acquisition Systems.

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REFERENCES

Alouani, A.T. and A. Kamal, 2006. " Pulmonary Tumor Detection Using Respiratory Lung Sound," Proc. Cairo International Bioengineering Conference, Cairo, Egypt.

Altera DE2, 2006."Using the SDRAM Memory on Altera's DE2 board with Verilog Design".

Altera Quartus II, 2006. version 6.0 Handbook, Volume 4: SOPC Builder.

Bashir A., 2007. "Wave File Format." Internet: http:// technology.niagarac.on.ca/courses/ctec1631/WavFileFormat.html

Cohen, A. and Landsberg, D., 1984. "Analysis and Automatic Classification of Breath Sounds", IEEE Trans. Biomed. Eng., BME-31, pp. 585-590.

Cohen, A., 1986. Biomedical Signal Processing, CRC press, Boca Raton, FL.

Comet®,2007. portable EEG and PSG system.

Druger, O., 1973. The Chest: It's Sign and Sounds, Humetrics, Los Angles, CA.

Hartman, X., 2001.Cross Correlation in Signal, Sound and Sensation, New York. AIP, 346.

Kiyokawah, H., Yonemarum, M., Horie, S. et al, 1995. "Frequency Analysis of Crackles Recorded with a Stethoscope-Equipped Recorder", Nippon Kyobu Shikkan Gakkai Zasshi, 12, pp. 1341-1347.

Kraman, S.S. and Austrheim, D., 1983. "Comparison of Lung Sounds and Transmitted Sound Amplitude in Normal Men", Am. Res. Respir. Dis., 128, pp. 451-454.

Lehrer, S., 1989. Understanding Lung Sound, W.B. Saunders, Philadelphia, PA.

National Instruments, 2007. Data Acquisition Card for Laptops and PDAs, Internet: http://sine.ni.com/nips/ cds/view/p/lang/en/nid/13122.

Oavriely, N., 1996. "Analysis of Breath Sounds in Bronchial Provocation Tests" (editorial), Am. J., Respir. Crit. Care Med., 153, pp. 1469-1471.

Sadik C. Esener, 2006. "Flash memory cards. "Internet: http://ww.wtec.org/loyola/hdmem/01_01.htm#f01_01

Urquhart, R.B., McGee, J., Macleod, J.E., Banham, S.W. and Moran, F., 1981. "The Diagnostic Value of Pulmonary Sounds", A preliminary Study by Computer Analysis, Comput. Biol. Med., 11, pp.129-139.

Western Digital, 2007. "*Western Digital Caviar RE2 WD4000YR."* Internet: http://www.storagereview.com /articles/200510/WD4000YR_2.html.

Wolfson Microelectronics, 2006. WM8731/WM8731L, Production data, Rev 3.4.

Xilinx Inc. 2007. "The 65nm Virtex-5 SXT FPGA" Internet:http://www.Xilinx.com.